Stress-Aware Periodic Test of Interconnects

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Preprint

Stress-Aware Periodic Test of Interconnects

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Abstract— **Safety-critical systems have to follow extremely high dependability requirements as specified in the standards for automotive, air, and space applications. The required high fault coverage at runtime is usually obtained by a combination of concurrent error detection or correction and periodic tests within rather short time intervals. The concurrent scheme ensures the integrity of computed results while the periodic test has to identify potential aging problems and to prevent any fault accumulation which may invalidate the concurrent error detection mechanism. Such periodic built-in self-test (BIST) schemes are already commercialized for memories and for random logic. The paper at hand extends this approach to interconnect structures. A BIST scheme is presented which targets interconnect defects before they will actually affect the system functionality at nominal speed. A BIST schedule is developed which significantly reduces aging caused by electromigration during the lifetime application of the periodic test.**

Keywords: Periodic Test, Functional Safety, Hidden Interconnect Defect, Electro-Migration, Multi-frequency Test.

I. INTRODUCTION

Functional safety is a key concern in autonomous systems. In the automotive domain, for example, the ISO 26262 standard defines clear targets for test and reliability that drive research and development in the industry [Eychenne16] [Nardi19] [Pateras17]. First of all, the manufacturing test must ensure a high product quality by reducing test escapes to a minimum ("zero defect strategy"). During operation, safety critical systems are typically protected by error correcting codes and other techniques for concurrent testing. However, safety-critical systems, such as anti-blocking brakes, may also have longer idle time, where faults cannot be detected by concurrent testing. Similarly, stand-by spare parts are not used during normal operation, but their health status must be maintained. To avoid fault accumulation during idle times, built-in tests are needed which can be triggered periodically. For logic circuits, quite a few approaches are already available addressing these specific requirements. They range from dedicated BIST and observation schemes [Liu18] [Mukherjee19] to applications of software-based self-test [Reimann14] [Bernardi16]. Similarly, schemes for embedded memories rely on scrubbing [Mariani05] and periodic consistency checking [Hellebrand02] in addition to the protection by the error detecting and correcting codes.

However, in today's complex systems, the reliability of the long interconnects between the components has also become a major concern. The severe impact of technology scaling on the signal integrity in bus structures or network on chip (NoC) links [Caignet01] has triggered research on advanced interconnect testing. Here specific defect and aging mechanisms such as crosstalk or electromigration (EM) must be addressed, which can manifest themselves for example as delay fault or glitches at the gate level. In this context, the BIST and monitoring schemes proposed in [Bai00] [Nourani01] [Pendurkar01] [Chen02] [Sekar02] [Tehranipoor03] [Tehranipoor04] [Grecu06] [Nourmandi-Pour10] [Sadeghi-Kohan12] [Mohammadi14], focus on manufacturing test, but they do not address the requirements and challenges of health monitoring during the lifetime. Nevertheless, because of the complex interplay between EM and crosstalk, periodic testing of interconnects is mandatory and at the same time extremely challenging. On the one hand, EM may change the interconnect geometry and lead to increased crosstalk effects. On the other hand, the crosstalk-induced currents can in turn aggravate EM [Livshits12], and even small crosstalk effects can constitute reliability risks that must be considered [Sadeghi-Kohan20].

The available interconnect BIST schemes for manufacturing testing cannot be directly applied, because they mainly target "large" crosstalk effects which change the system data. Furthermore, each test execution itself adds stress to the interconnects. In periodic testing, this stress can accumulate and lead to accelerated aging. Consequently, in a safety critical system, where a reliability above a given threshold has to be guaranteed, the test must be carefully designed to minimize its negative impact on the mission time. In particular, in the case of stand-by spare parts, a sufficient mission time after a reconfiguration must be ensured.

Degradation caused by EM has been studied extensively in the context of chip design [Black69a] [Black69b] [D'Heurle71] [Doyen08] [Mishra15], and EM-aware design techniques exploit self-healing mechanisms triggered by reversed current [Lienig18]. In particular, work on EM-aware routing in NoCs addresses the problem of stress accumulation by packet transmission over the network links [Hosseini11]. To exploit self-healing by a reversed current, a dynamic routing strategy balances the number of packets that are sent and received over a link. Such an EM-aware routing scheme can easily be combined with test and diagnosis schemes for NoCs reusing the NoC infrastructure [Grecu06] [Schley17].

In this paper, a new approach for periodic EM-aware test will be presented, which is applicable to general bi-directional

interconnect structures at the system level. It can identify and classify reliability risks before they actually cause a failure. At the same time, the proposed EM-aware strategy maximizes the mission time of the system. Similar to the dynamic routing strategy in [Hosseini11], it tries to properly balance senders and receivers during test. The scheme is based on a multi-frequency test, which not only detects failures, but also provides a reliability profile of the interconnect structures. The periodic update of this reliability profiles supports a dynamic test scheduling, where the direction of the test is changed whenever the accumulated stress gets too high.

Before the proposed strategy is explained in more detail, the necessary background is provided in Section II. Subsequently, Section III analyzes the impact of the periodic test on electromigration. Section IV introduces the basic BIST architecture. Finally, Section V deals with the proper tuning of this architecture and explains the developed concepts for test scheduling. The experimental results in Section VI will show that the developed stress-aware test improves the mission times by orders of magnitude compared to a straightforward approach.

II. Background

This section briefly summarizes the necessary background on interconnect modeling and test, the relation between coupling and electromigration, as well as the multi-frequency test scheme introduced in [Sadeghi-Kohan20].

A. Interconnect and Fault Modeling

Interconnect lines will be modeled as a sequence of RLC circuits [Chen98] [Cuviello99] [Roy09]. As an example, Figure 1 shows one segment of a three-lines interconnect. Each wire i is characterized by its capacitance to other layers C_i, inductance L_i, and resistance R_i. Between every two wires i and j, there are also coupling capacitances C_{ij}, inductances L_{ij}, and resistances R_{ij} depending on the space between the wires.
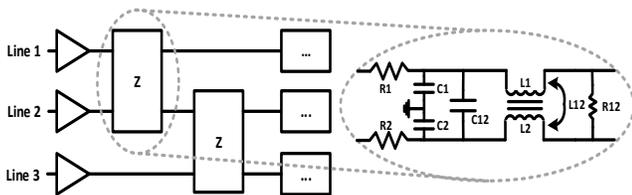
Figure 1. Model for on-chip communication [Cuviello99].

Coupling between lines leads to crosstalk effects such as glitches, delay and speedy faults, and also overshoots and undershoots. The amplitudes of glitch distortions and of the overshoots and undershoots as well as the delay sizes depend on the strength of the coupling elements.

Crosstalk effects are usually described as a signal distortion on a *victim line* caused by a transition on one or more *aggressor lines*. Several fault models have been proposed to support crosstalk analysis and test at higher levels of abstraction. The maximum aggressor (MA) model assumes that the worst-case effect on a single victim line is provoked when all other lines act as aggressors in the same way [Cuviello99].

However, this model does not consider the impact of inductances and does not always correctly reflect the worst case. To overcome the disadvantages of the MA model, some authors suggest to use pseudo-random patterns for signal integrity test [Nourani01]. Nevertheless, shorter test times can be ensured with advanced deterministic approaches. The maximum transition (MT) fault model combines a transition or a stable signal on a victim line with multiple transitions on a limited number of aggressor lines [Tehranipoor03]. Based on the analysis of the combined effect of capacitances and inductances, the maximal dominant signal integrity (MDSI) fault model also works with a limited number of aggressors but derives conditions for the remaining lines in addition to that [Chun07].

The MDSI model allows for a very simple deterministic test with only a few pattern pairs. Table 1 summarizes the necessary pattern pairs for a complete crosstalk test of one victim line. To test the victim for delays, glitches, and speedy faults, 6 pattern pairs are sufficient. As the MDSI fault model assumes that only one victim at a time is addressed, in total $6 \cdot N$ (possibly overlapping) pattern pairs are needed for an N-bit interconnect.

Table 1. Complete MDSI test of one victim line

Cross talk fault	Victim line	Aggressor lines	Other lines
Delayed transition	$0 \to 1$	$1 \to 0$	$0 \to 1$
	$1 \to 0$	$0 \to 1$	$1 \to 0$
Glitch	0	$0 \to 1$	$1 \to 0$
	1	$1 \to 0$	$0 \to 1$
Speedy transition	$0 \to 1$	$0 \to 1$	$0 \to 1$
	$1 \to 0$	$1 \to 0$	$1 \to 0$

A more efficient test scheme based on multiple victim testing (MVT) is proposed in [Nourmandi-Pour10] and used in this paper. The conditions for the signals on the victim and aggressor lines are the same as in the MDSI model, and working with several victim lines has a similar effect as the conditions for the remaining lines in the MDSI model. An example is shown in Figure 2, where the two victim lines v1 and v2 (blue lines) are tested in parallel for crosstalk delays by activating the inverse transitions on the neighboring aggressor lines (red lines).
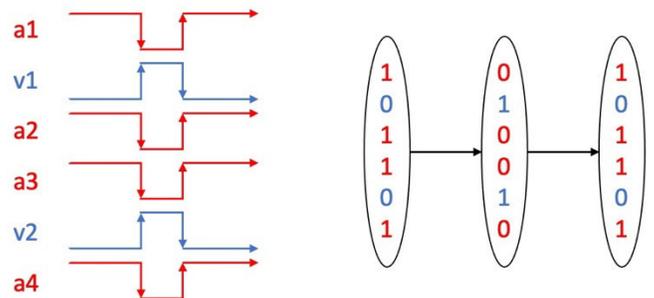
Figure 2. Test for crosstalk delays

2

B. Interconnect BIST

While many existing schemes for interconnect BIST rely on a serial transmission of test data within a boundary scan environment, the presented work deals with the parallel test application in SoCs. The short overview in this section therefore focuses on the main ideas and skips details on boundary-scan integration.

Early approaches on interconnect BIST mainly address manufacturing defects modeled as shorts, stuck-opens, and stuck-at faults [Hassan88]. Counter sequences, walking ones, or LFSR-based pseudo-random sequences are generated serially by respective test pattern generators.

With the increasing progress in technology, interconnect performance and signal integrity have become predominant. Bai et al. describe an approach for generating deterministic patterns based on the MA model [Bai00]. A small finite state machine produces the proper transitions for the victim line and the aggressor lines, which are then distributed to the interconnect via multiplexers. Sekar and Dey also base their analysis on the MA model but suggest to re-use the LFSR typically available for logic BIST [Sekar02]. To guarantee a high fault coverage with an acceptable number of patterns the LFSR-outputs are modified by some extra logic. In [Chen02] a software-based self-test relying on MA patterns is proposed.

To avoid the problems related to the MA model, an LFSR is used as a pseudo-random pattern generator in [Nourani01]. Furthermore, special receiver cells for interconnect BIST based on sense amplifiers are presented. Similarly, Pendurkar et al. build on small pre-characterized LFSRs which are combined to mimic the switching activity of the interconnect in system mode [Pendurkar01]. Other authors promote a pseudo-exhaustive test, where all possible combinations of transitions are applied to groups of lines, or even an exhaustive test, in case the interconnect topology is unknown [Liu07] [Rudnicki09]. Both approaches use LFSRs for pattern generation. Deterministic approaches for advanced fault models integrate tests based on the MT and the MDSI model [Tehranipoor04] [Mohammadi14].

A parallel BIST scheme for testing manufacturing defects is presented in [Jutman04]. It uses a simple circular shift register as the core of a parallel BIST scheme. In section IV a parallel generator for the periodic crosstalk test will be introduced for multiple victim test.

C. Reliability Measures

In this work the specification and evaluation of reliability properties relies on common fault tolerance concepts and terminology. As a more in-depth introduction is beyond the scope of this paper, the reader is referred to respective textbooks, e.g. [Koren07].

The reliability R(t) is formally defined as the probability that a system survives from time 0 to t. For safety critical systems, it is typically required that $R(t)$ is above a given threshold R_{th}, and the mission time $T_M(R_{th})$ is defined as time span where $R(t) \geq R_{th}$ holds. Changes in the design or test strategy are then evaluated by the mission time improvement factor

$$MTIF = T_M^{new}(R_{th})/T_M^{old}(R_{th}). \qquad (1)$$

If the mission times cannot be determined directly, they can be computed with the help of the median time to failure t50 or the more common mean time to failure MTTF as shown in the following.

If a constant failure rate λ is assumed, then

$$R(t) = e^{-\lambda t}, \text{ and } MTTF = \frac{1}{\lambda} \qquad (2)$$

hold [Koren07]. The median time to failure is the time when 50% of the interconnects fail, i.e. the reliability is $R(t_{50}) = 1/2$. Using Equation (2), it can be shown that

$$t_{50} = MTTF \cdot ln\,(2), \qquad (3)$$

And similarly

$$T_M = -MTTF \cdot l\,n(R_{th}) = -\frac{t_{50}}{ln(2)} \cdot ln\,(R_{th}). \qquad (4)$$

Therefore, the mission time improvement can also be estimated as

$$MTIF = \frac{MTTF^{new}}{MTTF^{old}} = \frac{t_{50}^{new}}{t_{50}^{old}}. \qquad (5)$$

D. Coupling and Electromigration

As shown in [Livshits12], crosstalk can aggravate EM and thus reduce the reliability of the system. This is not only true for crosstalk effects actually changing the functionality of the system [Sadeghi-Kohan20]. Even if the crosstalk noise only leads to small delays within the design margin, it can trigger EM. Such small crosstalk faults remain undetected by tests at the nominal frequency and are therefore called *hidden interconnect defects*.

The relation between coupling and EM, in particular in the presence of variations in the line spacing, will be summarized in the following. EM refers to the transportation of metal ions caused by an electrical field. For a detailed introduction into various aspects of EM in integrated circuit design, the reader is referred to the textbook of Lienig and Thiele [Lienig18]. The metal ion transport is reshaping interconnect lines over time. This, in turn, changes the resistance of interconnects and can lead to increased interconnect delays [Mishra15]. Furthermore, several studies have shown that EM can cause serious failures by creating hillocks and voids in the interconnect lines [Doyen08]. In the worst case, a hillock can become a bridging fault between adjacent wires, and a void can result in a broken line.

The impact of EM on the system is typically characterized by the median time to failure t_{50}. According to Black's Formula, t_{50} measured in hours can be estimated based on the physical parameters of the system as

$$t_{50} = \frac{A}{j^n} e^{E_a/k_B \cdot T}, \qquad (6)$$

where A is a constant depending on the cross-section of the wire, j is the current density in amperes per square centimeter, n is a constant related to the material, E_a is the activation energy in electron volts, k_B is the Boltzmann constant

and T is the temperature in degrees Kelvin [Black69a] [Black69b] [Sapatnekar19] [Tu19]. The material constant n is typically between 1 and 2, e.g. 1.1 - 1.3 for copper and 2 for aluminum [Lienig18].

When the parameters j and T change, the mission time improvement is obtained as

$$MTIF = \left(\frac{j^{old}}{j^{new}}\right)^n exp\left(\frac{E_a}{k_B}\left(\frac{1}{T^{new}} - \frac{1}{T^{old}}\right)\right) \qquad (7)$$

By inserting Formula (6) into equation (5).

As equations (6) and (7) show, in addition to the temperature, the current density j has a major impact on EM effects and on the resulting changes in mission time.

For a given cross-section, the current density is defined as the amount of charge per unit time that flows through a unit area. It can be estimated by

$$j = \frac{I_{avg}}{W \cdot H}. \qquad (8)$$

The parameters W and H denote the width and the height of the wire, and I_{avg} is the average current. The average current I_{avg} can be determined by simulations or analytically, e.g. using the techniques in [Agarwal07] [Blaauw03]. In CMOS technology, the dynamic power is dominant, therefore the average current can be estimated as $I_{avg} = C \cdot V_{dd} \cdot f \cdot p$, where C is the capacitance of the wire, V_{dd} is the supply voltage, f is the clock frequency, and p is the switching probability [Abella10]. The current density is then obtained as

$$j = \frac{C \cdot V_{dd} \cdot f \cdot p}{W \cdot H}. \qquad (9)$$

As coupling effects strongly depend on the line spacing, a realistic analysis of the induced average current must take into account variations of the interconnect layout. For this, in [Sadeghi-Kohan20] variations in the line spacing have been analyzed ranging from 100 % down to 80 % of the nominal value. Simulation results for 80 % of the nominal line spacing in 32 nm technology have shown more than a 20 % increase of the coupling capacitance and more than a 7 % increase of the coupling inductance for typical crosstalk patterns. A line spacing below 80 % of the nominal value has not been considered, because this would result in large crosstalk faults which change the functionality of the system and could be easily detected.

Figure 3 summarizes the impact of variations in the wire spacing on the average current for the 32 and 45 nm technologies and a glitch pattern 000 → 101 applied to a 3-line interconnect (source voltage is 0.9 volt). The horizontal axis shows variations in the line spacing ranging from 100 % down to 80 % of the nominal value, and the vertical axis shows the increase in current for the glitch pattern relative to the situation with nominal line spacing.

It can be observed that the changes in current evolve almost linearly with the increasing coupling capacitances and inductances caused by a reduced line spacing. In particular, the curve for the 32 nm technology shows that already small variations in the line spacing can increase the current by almost 10 %, and their contribution to EM cannot be neglected. Therefore, both manufacturing and periodic in-system test must also address hidden interconnect defects to identify possible reliability threats, before they actually cause a failure.
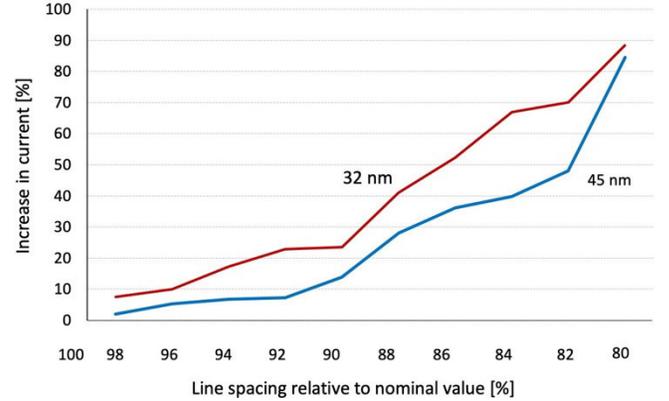
Figure 3. The average current increment for varying line spacing.

E. Dynamic Multi-frequency Test

As shown in Section II.C, already small variations in the line spacing have a non-negligible impact on EM. As the resulting crosstalk faults may be hidden at the nominal frequency, they must be tested at higher frequencies. The approach in [Sadeghi-Kohan20] uses several frequencies to characterize the risk of EM-degradation by crosstalk-induced delays. The main ideas are briefly summarized with the help of the pseudo-code in Figure 4.

```
Multi-frequency Test (L, F)
// Lines L
// Frequencies F = {f₀,…,fₘ}
i = 0;
while (L != {}) and (i < m)
   f = fᵢ;
   Lᵢ = test(L, fᵢ)
   L = L \ Lᵢ;
   i++
Return L₁, …, Lₘ;
```

Figure 4. Multi-frequency test.

The multi-frequency test starts with a delay test for all lines L at the nominal frequency $f_0 = f_{nom}$. In each iteration i, the frequency is increased to the next frequency f_i, and a delay test is applied to the remaining lines in L. The lines failing at f_i are collected in the set L_i and removed from the set of target lines L. These steps are repeated until the maximum frequency is reached or the list of target lines is empty.

The test time depends on the variations in the interconnect layout. If the line spacing is very narrow, then crosstalk delays will be observed on all lines already at the nominal frequency, and the test will stop after the first iteration. If the

line spacing is close to the nominal value for some lines, the test will go through all iterations until the hidden delays on these lines are detected by the highest frequency. In general, multi-frequency testing comes with severe challenges. Robust Adaptive Voltage & Frequency Systems (AVFS) are able to overcome them for the critical systems targeted in this paper. For interconnect lines the problem is simplified, as any distortion of the received signal is considered as a detected error.

After the test, each line is associated with the failing frequency as a measure of the severity of the fault. The lowest frequency detecting a delay can be used as a reliability indicator for the complete interconnect structure. This way, the test also monitors the health status of the system interconnects.

III. AGING AND HEALING

To predict reliability risks before an actual failure occurs, the reliability profile obtained by the multi-frequency test of Section II.E should be continuously updated by periodic tests, which in turn adds stress to the system, where the interval between tests is in the range of milliseconds. Although the stress induced by a single test may be negligible, the accumulated EM-degradation over the lifetime of a system is a serious issue in periodic testing. For EM-aware testing, possible self-healing effects must, therefore, be properly exploited as it is already done in EM-aware design [Lienig18].

Self-healing occurs when the current is reversed, because then also the direction of the ion transport is changed [Tao93]. This effect occurs when the direction of communication is changed or when inverse transitions lead to alternating current (AC) on the line. However, two complementary transitions will not lead to perfect healing, since the healing effects also depend on the severity of already caused damages and thus on the time between changes [Tao94] [Tao95]. The resulting difference between the opposite current densities is referred to as the *effective current density* in the sequel. For a more precise analysis of healing in the case of bidirectional communication or alternating current, in [Tao95] a healing parameter γ has been introduced. The effective current density for EM is given by

$$j_{ac} = j_{dc}^+ - \gamma \cdot j_{dc}^-, \qquad (10)$$

where j_{dc}^+ and j_{dc}^- are the average absolute values of the current densities in the forward and backward transition, or in the positive and negative half-cycle, respectively. The parameter γ depends on the frequency f

$$\gamma = 1 - 2\left(\frac{f_0}{f}\right)^{1/n}, \quad f_0 = \frac{1}{2 \cdot t_{50}(DC)}. \qquad (11)$$

Here, $t_{50}(DC)$ denotes the median time to failure for direct current (DC) in Eq. (6), and n is again the material constant in Black's formula. Furthermore, f_0 is the frequency where interconnects fail before the current is reversed. As self-healing is not possible in such a case, the formula is only valid for $f > f_0$.

Consequently, the median time to failure under AC stress is given by

$$t_{50}(AC) = \frac{A}{\left(j_{dc}^+ - \gamma j_{dc}^-\right)^n} \cdot e^{E_a/k_B \cdot T}. \qquad (12)$$

Based on Eqs. (10) to (12) the EM-degradation during test can be minimized following a similar strategy as it is described in [Hosseini11] for the communication in NoCs. In this work, it is assumed that j_{dc} is the nominal current density associated with the transfer of one data package. Furthermore, let m^+ denote the number of received packets, m^- the number of sent packets, and let $m \geq m^+ + m^-$ denote the total number of packets that can be sent over a link in case of 100 % utilization, then according to [Hosseini11] the average values j_{dc}^+ and j_{dc}^- in Eq. (10) can be estimated as

$$j_{dc}^+ = \frac{m^+}{m} \text{ and } j_{dc}^- = \frac{m^-}{m}. \qquad (13)$$

In case $m > m^+ + m^-$, the frequency f, which determines γ, must be adjusted by

$$f = f_{sys} \cdot \frac{m^+ + m^-}{m}, \qquad (14)$$

where f_{sys} denotes the frequency of the system clock. To minimize t_{50} for the communication links in the NoC, the authors suggest a dynamic routing scheme balancing sent and received packets on each link.

In the context of the periodic test for bidirectional interconnect structures, both alternating transitions during a single test and changing the direction of the test application contribute to self-healing. As expected, preliminary simulation results have shown that alternating transitions in a single test do not fully compensate each other, because the induced currents are not symmetric. This effect is even more pronounced in the presence of layout variations.

Because of the unpredictable impact of layout variations, it is not possible to exactly determine the current density of a single test upfront. Nevertheless, for minimizing the EM degradation by the periodic test over the lifetime of the system, a rough guideline can be established as in [Hosseini11]. The "forward" and "backward" test applications should be balanced for each interconnect section. The estimations in formula (13) will be even more precise in this case, since the test packets sent in both directions are identical. In addition to that, the test should dynamically adjust to the currently observed reliability profile and change the direction whenever needed.

IV. PATTERN GENERATION AND EVALUATION

This section introduces the basic BIST scheme for the proposed interconnect test. To simplify explanations, stress and recovery conditions are not considered yet. They will be in the focus of Section V. As pointed out in Section II.A, this work is based on multiple victim testing [Nourmandi-Pour10], where several victim lines are tested simultaneously and the transitions on victim and aggressor lines are generated as described in Table 1. Furthermore, a high-speed interconnect test at multiple frequencies is supported by parallel generation and application of test patterns.

1 Using the pattern pairs in Table 1 leads to a very regular
2 structure of the test. As the multi-frequency test of Section
3 II.E only targets crosstalk delays, one victim can be tested by
4 three test patterns with transitions $1 \rightarrow 0 \rightarrow 1$ on the victim
5 line and the opposite transitions $0 \rightarrow 1 \rightarrow 0$ on the aggressor
6 lines. As illustrated in Figure 5, a complete test for several
7 victims at a time can for example start with a '1' at all victim
8 lines and a '0' at all aggressor lines. The next two patterns
9 are obtained by bitwise inversion, such that the third pattern
10 is equal to the initial pattern.

Pattern 1	0 0 1 0 0 1 0 … 1 0 0
Pattern 2	1 1 0 1 1 0 1 … 0 1 1
Pattern 3	0 0 1 0 0 1 0 … 1 0 0
Pattern 4	1 0 0 1 0 0 1 … 0 1 0
Pattern 5	0 1 1 0 1 1 0 … 1 0 1
Pattern 6	1 0 0 1 0 0 1 … 0 1 0

11 …

12 Figure 5. Generating patterns for crosstalk delays.

13 To change the positions of victims, this pattern must be
14 shifted before again bitwise inversions are applied. In the
15 example, a complete test for crosstalk delay can be done with
16 9 patterns. In general, if $2 \cdot k$ aggressors are assumed per vic-
17 tim (k on each side), then $(k + 1) \cdot 3$ test patterns are suffi-
18 cient. Similarly, crosstalk glitches and speedy faults can be
19 tested by properly selecting the seeds and the positions for
20 bitwise inversions.

21 This can be implemented using the hardware structure shown
22 in Figure 6. The test starts with loading the appropriate seeds
23 into the pattern register the inversion register. Then, transi-
24 tions are generated until all necessary transitions have been
25 applied to the addressed victims. The set of victims can be
26 updated by simply shifting the registers and reseeding proper
27 seed bits to bit position 1.
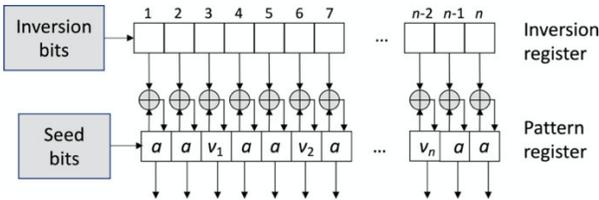
28

29 Figure 6. Generator for parallel multiple victim testing.

30 This simple structure is sufficient to implement the proposed
31 periodic multi-frequency test. If a more comprehensive test
32 is needed for the manufacturing test, it can also generate
33 patterns for glitch or speedy faults by properly adjusting the
34 seed and inversion bits. At only a little extra cost, this
35 generator can be extended, such that the pattern register
36 receives the first bit from a circular or a linear feedback (cf.
37 Figure 7). This way, the hardware can also be used for testing
38 static defects as in [Jutman04] or for an extended LFSR-
39 based signal integrity test as described in section II.B.

40 As already suggested in [Bai00], test response evaluation
41 will be based on pattern generation in the receiver. An iden-

42 tical generator will produce exactly the same set of test pat-
43 terns in the receiver, and the received patterns will be com-
44 pared to the expected ones.
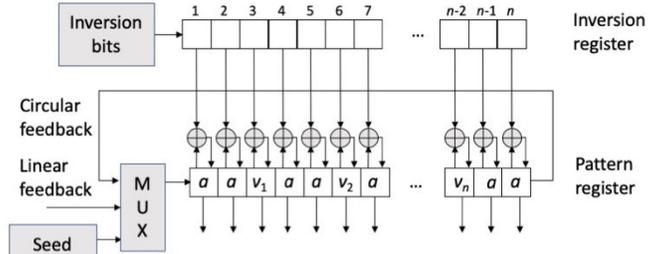
45

46 Figure 7. Extended generator for manufacturing and periodic test.

47 V. TEST TUNING AND SCHEDULING

48 In this section, it is shown how the basic BIST scheme of
49 Section IV can be used within the framework of a stress-
50 aware periodic test. For this, various implementation details
51 are discussed. In particular, a strategy for scheduling the tests
52 is presented, such that self-healing is supported.

53 *A. Use of Multi-frequency Test*

54 As pointed out in Section III, the EM-aware test must be
55 dynamically adapted to the current reliability profile of the
56 interconnect. For this, the multi-frequency test summarized
57 in Section II.E provides an effective solution. A frequency
58 sweep from the lowest to the highest frequency not only
59 reveals all crosstalk faults but also characterizes each line
60 with the failing frequency. Consider for example the inter-
61 connect layout with variations of Figure 8, where the per-
62 centages between the lines show the line spacing relative to
63 the nominal line spacing. If the manufacturing test is run with
64 ten different frequencies F_0 to F_9, then crosstalk delays due
65 to narrow line spacing (80 %) are already detected with the
66 lowest frequency F_0, whereas the highest frequency F_9 is
67 needed for close to nominal line spacing (98%), and for the
68 remaining lines, the intermediate frequency F_5 is sufficient.
69 Overall, the profile of the interconnect is described by the
70 line sets $L(F_0) = \{L_7, L_8, L_9, L_{10}\}$, $L(F_5) = \{L_6, L_5, L_4\}$, and
71 $L(F_9) = \{L_1, L_2, L_3\}$.
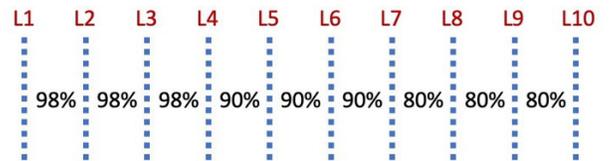
72

73 Figure 8. A sample layout of a 10-line interconnect

74 This profile is stored on-chip and can be compared to the new
75 profiles obtained during periodic testing. This way, aging
76 effects can be monitored and related to specific wires. This
77 information is then used to control mitigation schemes
78 [Abella08] or to adapt the test schedule, such that the stress
79 for critical wires is reduced.

Clock generation for the multi-frequency test can either re-use the existing infrastructure in circuits with dynamic volt-age and frequency scaling (DVFS), rely on existing schemes for on-chip clock generation in faster-than-at-speed test [Tayade08] [Pei10] [Pei15] or programmable delay elements [Sadeghi-Kohan17] [Liu18a] [Liu20].

B. Test Scheduling

Because of its regular structure, the basic BIST described in Section IV can be easily split into small chunks that fit into the slots provided for periodic testing. Small extensions of the test control are sufficient to ensure that the test can be stopped and resumed whenever needed, so that no special considerations for test scheduling are necessary in this respect. However, as explained in the following, proper test scheduling is crucial for minimizing the stress during the test.

According to Section III, properly balancing forward and backward test applications for each interconnect link is the main measure to support the self-healing of EM-degrada-tions. The test conditions in Table 1 naturally lead to a bal-anced distribution of rising and falling transitions. As explained in Section II.C, the self-healing effects depend on the frequency of changes and on the average positive and negative current densities. In a simple bidirectional intercon-nect between two cores, the main challenge is to find the best trade-off between a high frequency of changes and other test considerations.

In the more general scenario of Figure 9, the test patterns launched by one sender will reach multiple receivers, and it is not possible to simply revert this communication. But changing the sender with every test execution will also pro-vide some healing effects.
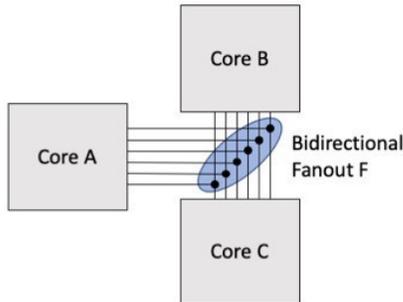
Figure 9. System interconnect with 3 cores.

This idea is analyzed for a simple rotating scheme in Table 2, where the communication on the interconnect sections (A, F), (B, F), (C, F) between the cores A, B, C, and the fanout F is shown. The first column counts the number of test executions, and the second column identifies the sender among the three cores A, B, C. The remaining columns symbolically show the direction of the current in the three interconnect segments between the bidirectional fanout F and the three cores A, B, C. It can be observed that changing the sender will compensate the stress on two interconnect segments but add stress to the remaining third segment.

Although the simple rotating scheme of Table 2 cannot fully avoid the accumulation of stress effects, its analysis also shows that the stress-recovery balance of a specific intercon-nect segment can always be improved by selecting a proper sender. This observation is exploited for dynamic test sched-uling as follows. In regular intervals, the reliability profile is checked, and the interconnect segment from F to the receiver X observing the largest faults is considered critical. The next sender is then determined based on the recorded sender/receiver information for X. If X has been used as a receiver in the majority of cases, then it is now used as a sender. If it has been mostly used as a sender, X now becomes a receiver.

Table 2. Example for rotating test schedule with 3 cores A, B, C and bidirectional fanout F as in Figure 9

Test	Sender	Current on Affected Intercon-nect Section		
		(A, F)	(B, F)	(C, F)
1	Core A	→	←	←
2	Core B	←	→	←
3	Core C	←	←	→
4	Core A	→	←	←
…				

VI.   EXPERIMENTAL RESULTS

To validate the presented technique, a simulation using HSPICE has been conducted. As the work addresses safety critical systems, a scenario has been assumed which is typical for automotive applications. Here high reliability thresholds have to be guaranteed even at extremely high temperatures. This is for example documented in the AEC Q100 Standard for accelerated aging tests [AEC21]. The highest quality "grade" defines a temperature spectrum from -40 °C to 150 °C. While the temperatures in the AEC Q100 standard refer to ambient temperatures, the temperature parameter T in Black's formula denotes the junction temperature. The junction temperature T is higher than the ambient temperature and can be derived by

$$T = T_a + P_{chip} \cdot R_{ja} \qquad (15)$$

where T_a denotes the ambient temperature, P_{chip} is the total power dissipation of the chip and R_{ja} is the junction-to-ambi-ent thermal resistance [Vassighi06]. Since the exact values for P_{chip} and R_{ja} were not available for the study, the range for T is assumed between 40 °C and 175 °C in the simulation study described in the following.

Furthermore, all experiments are based on a 32 nm tech-nology with the interconnect parameters list in Table 3. The interconnect structures are 32-bit wide in all experiments, and random layout variations are applied as illustrated in Figure 8. For the periodic test, a fixed timeline is assumed as sketched in Figure 10. The time intervals should be selected, such that self-healing is still possible for EM degradations. Furthermore, as degradations in the chip do not always evolve gradually at a slow pace, the time intervals for safety critical applications must be relatively short.

Table 3. Interconnect parameters in 32 nm technology

Parameter	Value or Range
Height (space between wire and reference plane)	0.09 μm
Width	84.4 nm
Height	151 nm
Space (nominal)	84.4 nm
Space variation factor	0.8 to 0.98
Length	2000 μm (100 μm distance between buffers)
Conductor resistivity for copper	1.7e-8 Ωm
Dielectric constant	1.36
Supply voltage	0.9 V
n	1.1 - 1.3
E_a	0.9

In our experiments, the time interval between two tests has been set to 0.25 ms, and during the test phase, a complete multi-frequency test with 10 frequencies is performed.
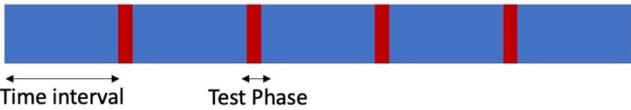
Figure 10. Periodic interconnect test timeline.

For the proposed BIST scheme, the number of patterns for a single frequency is $(k + 1) \cdot 3$, where k is the number of aggressors on each side of the victim. Consequently, the overall number of test patterns is between $(k + 1) \cdot 3$ and $10 \cdot (k + 1) \cdot 3$ (cf. Section IV). In our experiments, the parameter k has been set to $k = 2$ and $k = 4$. As we assume that all 10 frequencies are used in each test, 90 patterns must be applied for $k = 2$, and 150 for $k = 4$.

The simulation study covers both a simple interconnects between two cores A and B and the interconnect structure of Figure 9. Overall, the experiments analyze the test strategies listed in Table 4.

Since the main motivation for the periodic BIST is to avoid fault accumulation during longer idle times, the presented analysis focuses on stress and self-healing the during test and does not take into account self-healing effects during normal system operation.

A. Simple interconnects

In this subsection, only simple interconnects are considered, and the strategies *One_directional* and *Bi_directional* are compared to each other for $k = 2$. As explained above, potential healing effects by data transfers between the tests are neglected. In the first step the current densities, the median times to failure t_{50}, and the mission times T_M for a reliability threshold $R_{th} = 0.999999$ have been determined for the one-directional test.

Table 4. Investigated test strategies

Strategy		Details
One_directional	A → B	Tests are applied always in the same direction
Bi_directional	A ⇄ B	Alternating test directions
Just_A	(diagram: A sender, B and C receivers)	A is always the sender. B and C are receivers.
Rotation	(diagram: rotating scheme A, B, C)	Rotating scheme of Table 2.

To obtain the respective values for the bi-directional test, the effective current densities introduced in Formula (10) have been determined based on the self-healing parameter γ. According to Formula (11), γ depends on the frequencies $f_0 = 1/t_{50}(DC)$ and f, and as the time between two tests is 0.25 ms in our experiments, the frequency f is set to 2 KHz.

The observed current densities are independent of the temperature in the one-directional case and reach 3139 A/cm2. In the bi-directional test, the current densities are reduced by two orders of magnitude. Although they are temperature dependent because of the self-healing parameter γ, the changes are extremely small and the values range between 62 and 63 A/cm2.

The results for median times to failure t50 and the resulting mission times TM in years are summarized in Table 5. The columns 2 and 3 show t50 for both test strategies, and the mission times are reported in columns 4 and 5. Finally, the mission time improvement factor MTIF is listed in column 6. According to Formula (7), the mission time improvement only depends on the current densities and the parameter n for a fixed temperature, which explains that this parameter does not change over the temperature range.

Although the median times to failure in columns 2 and 3 are extremely high, the mission times in columns 4 and 5 quickly decrease over the temperature range because of the high reliability threshold for safety critical systems. For example, for the one-dimensional test the mission time at 125 °C is below 1.5 years, and for 150 °C it is already below 4 months (0.31 years). But the self-healing effects triggered by the bi-directional test application can ensure considerably higher mission times (MTIF ≈ 74). For example, the mission time at 150 °C is improved from approximately 4 months to more than 23 years.

As shown in Table 6, this effect is even more pronounced, if the worst-case value 1.3 is assumed for the parameter n. Here the mission time for the one-directional test at 150 °C is already below one month (0.06 years).

Table 5. Mission Times for One-directional and Bi-directional Test, n = 1.1, and k = 2
(Current densities are 3139 A/cm^2 for One_dir and 62 - 63 A/cm^2 for Bi_dir).

(1) Temperature	t_{50} [years]		Mission Time T_M (0.999999) [years]		(6) MTIF
	(2) One_dir	(3) Bi_dir	(4) One_dir	(5) Bi_dir	
40 °C	1,256,322,005	67,231,850,134,437	1,812.49	134,715.36	74.3
55 °C	273,659,613	14,644,845,786,190	394.81	29,344.51	74.3
65 °C	106,800,588	5,715,414,563,517	154.08	11,452.22	74.3
75 °C	43,995,813	2,354,428,135,529	63.47	4,717.67	74.3
85 °C	19,043,970	1,019,134,655,764	27.47	2,042.08	74.3
95 °C	8,626,992	461,671,892,875	12.45	925.07	74.3
105 °C	4,075,207	218,083,963,268	5.88	436.98	74.3
115 °C	2,000,888	107,077,115,625	2.89	214.56	74.3
125 °C	1,018,155	54,486,343,169	1.47	109.18	74.3
150 °C	216,254	11,572,745,964	0.31	23.19	74.3
175 °C	54,599	2,921,816,617	0.08	5.85	74.3

Table 6. Mission Times for One-directional and Bi-directional Test, n = 1.3, and k =2
(Current densities are 3139 A/cm^2 for One_dir and 62 - 63 A/cm^2 for Bi_dir).

(1) Temperature	t_{50} [years]		Mission Time T_M (0.999999) [years]		(6) MTIF
	(2) One_dir	(3) Bi_dir	(4) One_dir	(5) Bi_dir	
40 °C	251,045,731	29,405,876,606,661	362.18	58,921.82	162.7
55 °C	54,684,288	6,405,352,458,728	78.89	12,834.68	162.7
65 °C	21,341,526	2,499,796,619,469	30.79	5,008.95	162.7
75 °C	8,791,503	1,029,769,273,309	12.68	2,063.39	162.7
85 °C	3,805,478	445,739,972,966	5.49	893.15	162.7
95 °C	1,723,895	201,918,234,454	2,49	404,59	162.7
105 °C	814,331	95,378,900,383	1.17	191.11	162.7
115 °C	399,828	46,827,694,797	0.58	93.83	162.7
125 °C	203,453	23,826,346,903	0.29	47.74	162.7
150 °C	43,213	5,058,257,698	0.06	10.14	162.6
175 °C	10,910	1,275,449,638	0.02	2.56	162.4

Since the mission time improvement grows with the parameter *n* according to Formula (7), the bi-directional test can still ensure a reasonable mission of more than 10 years.

The highlighted trends are illustrated in Figure 11, where the mission times for *n* = 1.3 are shown as a function of temperature in a logarithmic scale. The blue line corresponds to the one-directional without self-healing, and the orange line to the bi-directional case with self-healing.

It can be seen that the curves have more or less the same shape, which is in line with the almost constant mission time improvement factor.
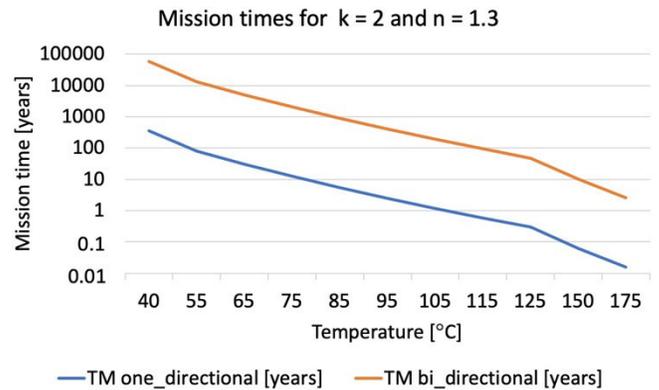

Figure 11. Mission times for one- and bi-directional test.

Table 7. Comparing Mission Times for k = 2 and k = 4, n = 1.3.

(1) Temperature	T_M (0.999999) one_directional [years]		T_M (0.999999) bi_directional [years]		MTIF	
	(2) k = 2	(3) k = 4	(4) k = 2	(5) k = 4	(6) k = 2	(7) k = 4
40 °C	362.18	270.98	58,921.82	43,094.73	162.7	159.0
55 °C	78.89	59.03	12,834.68	9,387.14	162.7	159.0
65 °C	30.79	23.04	5,008.95	3,663.49	162.7	159.0
75 °C	12.68	9.49	2,063.39	1,509.14	162.7	159.0
85 °C	5.49	4.11	893.15	653.24	162.7	159.0
95 °C	2.49	1.86	404.59	295.91	162.7	159.0
105 °C	1.17	0.88	191.11	139.78	162.7	159.0
115 °C	0.58	0.43	93.83	68.63	162.7	159.0
125 °C	0.29	0.22	47.74	34.92	162.7	159.0
150 °C	0.06	0.05	10.14	7.41	162.6	158.9
175 °C	0.02	0.01	2.56	1.87	162.4	158.7

Table 8. Mission Times for the Strategies Just_A and Rotation, n = 1.3 and k = 4
(Current densities are 5100 A/cm² for Just_A and 93 A/cm² for Rotation).

(1) Temperature	t_{50} [years]		Mission Time T_M (0.999999) [years]		(6) MTIF
	(2 Just_A	(3) Rotation	(4) Just_A	(5) Rotation	
40 °C	96,155,905,716	17,601,569,003,957	192.67	35,269.02	183.1
55 °C	20,945,256,894	3,834,073,234,943	41.97	7,682.50	183.1
65 °C	8,174,263,024	1,496,312,255,688	16.38	2,.998.23	183.1
75 °C	3,367,334,630	616,393,196,239	6.75	1,235.09	183.1
85 °C	1,457,579,825	266,808,788,527	2.92	534.62	183.0
95 °C	660,289,074	120,863,515,232	1.32	242.18	183.0
105 °C	311,906,364	57,091,825,547	0.62	114.40	183.0
115 °C	153,142,908	28,030,291,720	0.31	56.17	183.0
125 °C	77,926,909	14,262,232,281	0.16	28.58	183.0
150 °C	16,551,367	3,028,031,835	0.03	6.07	182.9
175 °C	4,178,733	763,663,990	0.01	1.53	182.8

The same experiments have been repeated for k = 4 where 4 aggressors are assumed on each side of the victim line and a higher number of test patterns are needed. Table 7 compares the mission times and the mission time improvement factors for n = 1.3 to the previously discussed case of k = 2. As expected, the longer test times for k = 4 result in a higher stress and reduced mission times.

But also in this case, the bi-directional test provides a mission time improvement factor of 159 and still ensures a mission time for more than 7 years at 150 °C.

B. General interconnect structures

This subsection focuses on more general interconnect structures and presents the results for strategies *Just_A* and *Rota-tion*. As the basic trends are the same as discussed in Subsection VI.A, only the worst-case results for *n* = 1.3 and *k* = 4 are reported in Table 8.

Again, the straightforward test application *Just_A* is associated with an unacceptable reduction of the mission times at higher temperatures. The self-healing effects introduced by the *Rotation* scheme lead to a mission time improvement by orders of magnitude. For example, at 150 °C, the *Rotation* strategy still guarantees a mission time of 6 years. For the more optimistic scenario with k = 2 and n = 1.1, the mission time would even increase to more than 19 years.

Plotting the mission times as a function of temperature (cf. Figure 12) shows the same general trends as in the case of simple interconnects in Figure 11. Now, the blue line

corresponds to using only one sender without self-healing, and the orange line to the rotation scheme with self-healing.
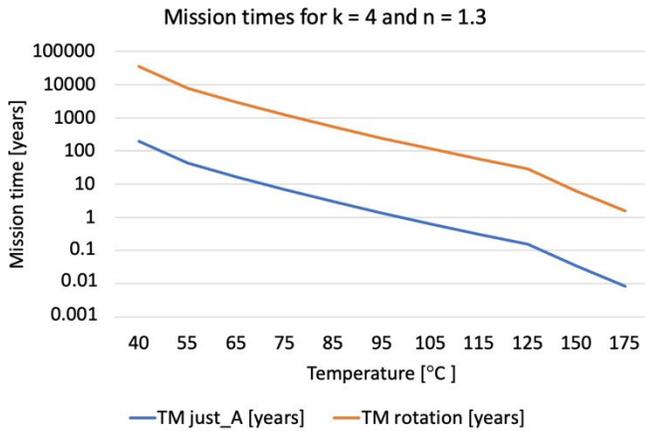
Figure 12. Mission times for general interconnects.

VII. CONCLUSIONS

Periodic interconnect testing is mandatory in safety critical systems to monitor components with longer idle times as well as standby spare units. However, the analysis in this paper has shown that a straightforward test strategy can lead to stress-induced electromigration and drastically reduce the mission time of the system. This effect gets extremely critical at higher temperatures which occur for example in the automotive domain. The proposed EM-aware strategy exploits self-healing effects triggered by reverse current. A bidirectional test for simple interconnects and a rotating test schedule for more complex interconnect structures improve the available lifetime for the system workload by orders of magnitude.

VIII. FUNDING

IX. CONFLICT OF INTEREST

The authors declare that they have no competing interests.

X. DATA AVAILABILITY

The datasets generated and analyzed during the current study are available from the corresponding author on reasonable request.

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