Diagnostic Test of Robust Circuits

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Abstract: Robust circuits are able to tolerate certain faults, but also pose additional challenges for test and diagnosis. To improve yield, the test must distinguish between critical faults and such faults, that could be compensated during system operation; in addition, efficient diagnosis procedures are needed to support yield ramp-up in the case of critical faults. Previous work on circuits with time redundancy has shown that "signature rollback" can distinguish critical permanent faults from uncritical transient faults. The test is partitioned into shorter sessions, and a rollback is triggered immediately after a faulty session. If the repeated session shows the correct result, then a transient fault is assumed. The reference values for the sessions are represented in a very compact format. Storing only a few bits characterizing the MISR state over time can provide the same quality as storing the complete signature. In this work the signature rollback scheme is extended to an integrated test and diagnosis procedure. It is shown that a single test run with highly compacted reference data is sufficient to reach a comparable diagnostic resolution to that of a diagnostic session without any data compaction.

Preprint

Diagnostic Test of Robust Circuits

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Abstract—**Robust circuits are able to tolerate certain faults, but also pose additional challenges for test and diagnosis. To improve yield, the test must distinguish between critical faults and such faults, that could be compensated during system operation; in addition, efficient diagnosis procedures are needed to support yield ramp-up in the case of critical faults. Previous work on circuits with time redundancy has shown that "signature rollback" can distinguish critical permanent faults from uncritical transient faults. The test is partitioned into shorter sessions, and a rollback is triggered immediately after a faulty session. If the repeated session shows the correct result, then a transient fault is assumed. The reference values for the sessions are represented in a very compact format. Storing only a few bits characterizing the MISR state over time can provide the same quality as storing the complete signature. In this work the signature rollback scheme is extended to an integrated test and diagnosis procedure. It is shown that a single test run with highly compacted reference data is sufficient to reach a comparable diagnostic resolution to that of a diagnostic session without any data compaction.**

Index Terms—Robust Circuits; Built-in Self-Test, Built-in Self-Diagnosis; Time Redundancy

I. Introduction

As parameter variations grow with each technology node, new robust and self-adaptive architectures have been developed. These techniques are able to handle errors during system operation and support the online calibration of system parameters such as supply voltage or frequency [1], [2], [3], [4]. The RAZOR processor, for example, can compensate delay and transient faults by means of additional shadow latches in the system registers [2], [3]. If the contents of the system flip-flops do not match those of the shadow latches, the processor pipeline state can be corrected and any corrupted computation can be restarted. Another technique for time redundancy is the GRAAL architecture, which features a level-sensitive design with two non-overlapping clocks [5]. Other approaches address, for example, the detection and compensation of aging effects [6], [7].

Robust architectures make it possible for system designers to take better advantages of the new process technologies. However, they also introduce new challenges for test and diagnosis. On the one hand, if only the functional inputs and outputs of a robust circuit are evaluated during test, critical defects may be masked out by the built-in error detection and correction mechanisms. On the other hand, structural test procedures relying on DfT can lead to unnecessary yield loss, if the test reveals failures that could be compensated during system operation. To allow an optimal interpretation of the test results and support yield ramp up, test procedures for robust architectures have to distinguish between critical and non-critical faults. For this purpose, an efficient interaction between test and diagnosis is necessary.

In [8] a BIST scheme based on the STUMPS architecture has been proposed for circuits with time redundancy [9]. This scheme can distinguish between transient and permanent faults and reduces the yield loss this way. The test is partitioned into N shorter sessions, and after each session the test result is compared to the corresponding reference result. For this comparison it is sufficient to store only a short bit sequence characterizing the state of the MISR over several time steps [10]. If the generated bit sequence does not match the expected response, then the current session is immediately repeated. If no fault is detected after the second run, the failure is attributed to a transient fault. Otherwise, the fault is considered to be permanent and the chip is classified accordingly.

Actually, another fault in the second run can be the result of either a permanent fault or an additional transient fault. In both cases a more precise diagnosis is important to improve the production process: an accumulation of transient faults may indicate a particularly susceptible structure in the circuit, while the presence of many permanent faults may indicate a problem in the manufacturing process.

This paper combines the signature rollback scheme developed in [8] and [10] with a procedure for direct diagnosis. This diagnostic technique is not confined to the stuck-at fault model and supports the diagnosis of a large variety of defect mechanisms [11]. In particular, it allows dealing with transient and intermittent faults. It is shown, that a single test run is sufficient to reach a diagnostic resolution comparable to that of a diagnostic procedure without response compaction.

The paper is structured as follows. In the following section the basics for the integrated test and diagnosis as well as the corresponding fault model are briefly summarized. Subsequently, in Section III the new integrated test and diagnosis procedure is introduced. Finally, in Section IV the experimental results are presented to validate the new scheme.

II. State of the Art

A. Signature Rollback

The signature rollback scheme is based on the STUMPS architecture sketched in Figure 1 [9]. It does not depend on any specific test pattern generator (TPG). To implement a random test, the TPG block may consist of a linear feedback shift register (LFSR) and a phase shifter. Any other more advanced pattern generator can be used for decompressing deterministic patterns, in which case, the corresponding seeds have to be stored on chip. The test responses are compacted by means of a multiple input shift register (MISR).

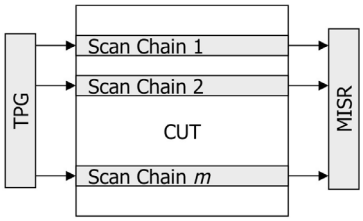

Figure 1: STUMPS-Architecture.

As described above, a given test T is partitioned into N shorter sessions $T_1, ..., T_N$ of equal length. At the end of each session T_j, the obtained signature in the MISR is compared to the reference signature. In case of a mismatch, the test is repeated immediately to distinguish transient from permanent faults. As shown in [8], for growing values of N the yield improvement increases and the test time decreases. But as N increases, the hardware overhead also increases due to the storage required for the reference data. The analytical model developed in [8] provides guidelines to adjust the parameters of the scheme, such that for a given failure rate λ the best trade-off between hardware overhead, yield improvement and test time is obtained.

The hardware cost can be reduced further by compacting the reference data. Instead of the full signature, for each session only a parity sequence is stored, which monitors the states of the MISR over several time steps [10]. Figure 2 shows the complete architecture for a mixed-mode test with random and deterministic patterns.

During test, the j-th session starts by storing the initial state of the MISR in the backup register so that a later restart of the session is possible. For deterministic patterns, the TPG is further initialized with the corresponding seed. When random test patterns are used, the TPG generates the next patterns without initialization, but the initial state of the TPG is stored in a backup register. At the end of a session, the MISR continues to run over the next l clocks and the obtained sequence of parity bits is compared to the reference data. As shown in [10], the test quality reaches a level comparable to an evaluation of the full signature already for small values of l, for example $l = 8$. This way, the storage amount of the necessary reference data can be reduced significantly. However, l additional clocks per session are required to calculate the parity sequence.

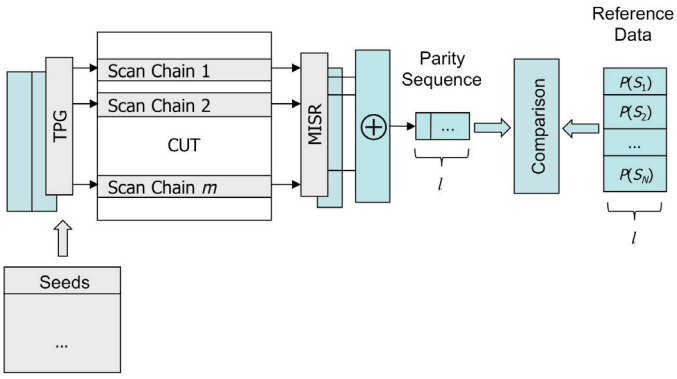

Figure 2: Signature rollback with an extreme compaction method using parity sequences [10].

When a failure occurs, the test is repeated after restoring the initial states of the TPG and MISR from the backup register or pattern memory.

B. Conditional Stuck-at Fault Model

In order to analyze arbitrary and complex defect mechanisms, especially transient faults, the conditional stuck-at fault model is applied [12]. For each line v, we consider the conditional stuck-at faults *cond*_0_v and *cond*_1_v. The condition *cond* describes arbitrary Boolean or timing properties, and if *cond* is met, the fault is active and the line is forced to either 0 or 1. For instance, (v=1)_0_v is a permanent stuck-at-0 fault, and (v_{-1}=0 ∧ v=1)_0_v describes a slow-to-rise fault. To describe transient faults, a particular pattern of a pattern sequence $P = (p_1, ..., p_n)$ is specified in *cond*. Assuming inputs $x = (x_1, …, x_s)$, the expression (x=p_i | P)_0_v means, that the line v is set to '0' by pattern p_i when the pattern sequence P is applied. This allows describing transient faults caused by test pattern combinations, for instance due to voltage drop or other dynamic parameter variations.

C. Built-In Diagnosis

Built-in self-diagnosis (BISD) has been studied intensively in the literature, and it is beyond the scope of this paper to give a complete review of the state of the art. Basically, logic diagnosis can follow one of two approaches. In indirect diagnosis, the failing signatures are analyzed and the logic values captured by the scan elements are computed

for each pattern in the pattern block. This procedure usually requires several test sessions [13], [14], [15], [16], [17], [18], [19]. Diagnosis algorithms for combinational logic can then be applied to the resulting failure information [20], [21], [22], [23]. In direct diagnosis, the fault location is identified directly from the faulty signature, without sorting out the values of each scan element [24]. However, this method still requires several test sessions and can only handle stuck-at faults or the techniques are incompatible with the STUMPS architecture [24], [25], [26].

In [11] a new approach for direct diagnosis has been proposed, which is based on the STUMPS architecture and requires only a single test session to achieve high fault coverage and diagnostic resolution for arbitrary defects. Similar to the signature rollback method described above, in this diagnostic procedure a test is partitioned into N test sessions T_1, ..., T_N. The diagnostic algorithm analyzes the intermediate signature of each test session and calculates an ordered list of possible defect locations, which are able to explain the defect behavior. The main ideas of the algorithm are briefly summarized below.

If in session T_j the observed signature $S_{obs}(T_j)$ differs from the reference signature $S_{ref}(T_j)$, then for every line v the conditional stuck-at faults

$$(x=p_1 \mid T_j)\_0\_v, \ldots, (x=p_n \mid T_j)\_0\_v$$

and

$$(x=p_1 \mid T_j)\_1\_v, \ldots, (x=p_n \mid T_j)\_1\_v$$

are analyzed, where x denotes the circuit inputs and p_1, …, p_n are the test patterns of a test session T_j. Every single fault $(x=p_i \mid T_j)\_0\_v$ or $(x=p_i \mid T_j)\_1\_v$ causes a divergence $d(p_i, 0)$ or $d(p_i, 1)$ from the reference signature, respectively. The values $d(p_i, 0)$ and $d(p_i, 1)$ can be precomputed and stored.

The linear equations

$$c_1 d(p_1, 0) \oplus \ldots \oplus c_n d(p_n, 0) = S_{obs}(T_j) \oplus S_{ref}(T_j)$$

and

$$c_1 d(p_1, 1) \oplus \ldots \oplus c_n d(p_n, 1) = S_{obs}(T_j) \oplus S_{ref}(T_j)$$

in the variables $c_1, \ldots, c_n \in \{0,1\}$ describe all possible conditions which explain the observed defect behavior at line v. That is, a fault at line v can be the single cause of the faulty behavior, only if the resulting system of linear equations is solvable. To have one unique solution for such a system, and therefore to perform more precise diagnosis, the number of variables n has to be less than or equal to the number of equations in the system. This means, the number of patterns in each test session has to be less than or equal to the number of bits in the MISR signature. If a solution is found for a given line v, this line is identified as a fault candidate. The number of test sessions, in which line v is a possible fault candidate, is used as a measure of the fault's evidence. The higher the evidence score is, the more likely the fault at line v is in fact the real cause of the defect behavior, and the higher is the ranking in the candidate list. If two faults explain the same number of test sessions, then the fault sensitized less often is considered the more likely candidate.

III. Integration of Test and Diagnosis

To implement a diagnostic test for robust circuits, both methods described above need to be combined in an efficient way. In this section, the necessary adjustments to the test infrastructure are explained in detail.

For both signature rollback, described in section II-A, and the diagnosis algorithm described in section II-C, the test is partitioned into test sessions T_1, ..., T_N. However, the diagnosis procedure works with the complete intermediate signatures, while signature rollback only evaluates a short sequence of parity bits. On the other hand, both additional hardware and test time are necessary for the signature rollback scheme: the parity logic requires some area on chip, and the calculation of the parity sequences requires l extra clocks at the end of each session. To integrate both methods into an efficient test and diagnosis procedure, the following adjustments are proposed.

To diagnose the sessions independently, the MISR is initialized to the all-zero state at the beginning of each session. The backup register, which was used for storing the initial state of the MISR, is replaced by a shadow MISR. At the end of each session, the calculated signature is transferred to the shadow MISR, which is then allowed to run free until the MISR has compacted the first pattern of the next session. This scheme offers the following benefits: firstly, in the fault-free case the test time corresponds to the regular test time of a standard test without the penalty for calculating the parity sequences. Secondly, the hardware overhead can be reduced, since the parity logic is no longer necessary. To show that the proposed scheme reaches the same quality as the solution relying on parity sequences in [10], the error propagation in a MISR is analyzed in some more detail in the following.

The state transitions of a MISR are linear transformations described by a matrix H as sketched in Figure 3. If an error $e = (e_0, \ldots, e_{k-1})$ occurs at time $t = 0$, the value $d^1 + e$ enters the MISR instead of d^1, and the sequence He, H^2e, H^3e, … describes the differences of the following states from the respective fault free states. This shows that the error propagation evolves like the state sequence of an autonomous linear feedback shift register (LFSR) with feedback polynomial $h(X)$ and initial state e. It is known from LFSR theory that the output sequence observed at a flip-flop x_i is a pseudo-random sequence, if $h(X)$ is a primitive polynomial. This means that the probability of detecting an error e at the output of a flip-flop x_i is ½. Accordingly, observing l state bits increases the probability of error detection to $1 - 2^{-l}$.

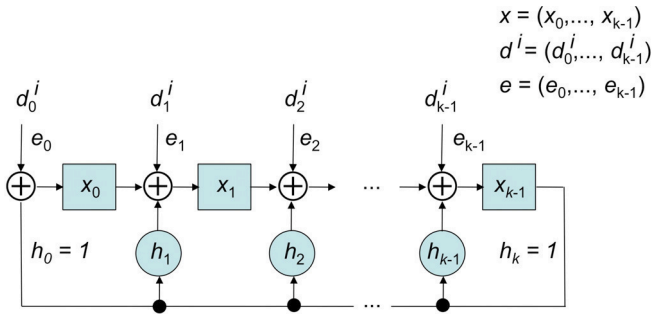

Figure 3: MISR.

Although the probability of error detection is already very close to 1 for small values of l, errors can still be masked in a worst-case scenario. For instance, if the state bits x_{k-1}, ..., x_{k-l} are observed and the error e first occurs in x_0, at least $k - l$ clocks are needed to observe this error. This problem was solved in [10] by the parity logic, which calculates the parity bits over all state bits of the MISR. However, as described above, the shadow MISR runs as long as the first pattern of the next session is completely compacted. Consequently, the architecture provides enough time for error propagation and, therefore, it is sufficient to observe l MISR bits in different time steps during the operation of the shadow MISR. Figure 4 shows the corresponding architecture.

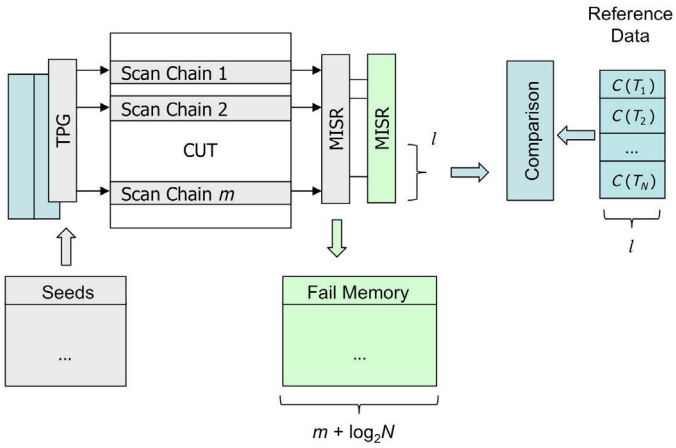

Figure 4: Architecture for the robust BIST with diagnosis.

In the resulting self-test architecture the parity logic is no longer needed and, therefore, the required hardware resources are reduced compared to those of the original signature rollback scheme. Similarly, the memory requirements for logic diagnosis are also reduced since the expected session signatures are further compacted into a few bits. As shown in the next section this can be done without any impact on the fault coverage. For logic diagnosis of critical faults the fail memory is still employed, which holds the full signatures and the number of the test sessions in which the errors occur.

IV. Experimental Results

In order to validate the integrated test and diagnosis method proposed in section III, several experiments with industrial circuits have been performed. Thereby the performance of the techniques in terms of fault coverage, hardware overhead and diagnostic resolution is quantified.

The relevant characteristics of the circuits, kindly provided by NXP, are listed in Table I.

TABLE I. Circuit characteristics

Circuit	*#Gates*	*#PPO*	*Scan Chains*	*Max. Length*	*# Stuck-at Faults*
p100k	84356	5829	270	53	162129
p141k	152808	10502	264	45	283548
p239k	224597	18495	260	61	455992
p259k	298796	18495	360	61	607536
p267k	239687	16621	260	62	366871
p269k	239771	16621	360	62	371209
p279k	257736	17835	385	59	493844
p286k	332726	17835	385	60	648044
p295k	249747	18521	330	62	472124
p330k	312666	17468	320	64	540758
p378k	341315	17420	325	64	816534

The first column shows the circuit name, and columns two to five indicate the number of gates, the number of pseudo-primary outputs, the number of scan chains k, and the length of the longest scan chain m. The last column shows the number of collapsed stuck-at faults.

As described in section III, only a short bit sequence is stored as reference data, instead of the full signature. For these experiments, the shadow MISR is simulated until the first pattern of the test session is completely compacted. Table II compares the fault coverage of stuck-at faults without any compaction to the proposed compaction scheme, where the number of observed state bits l was set to 8.

TABLE II. Pattern Set and Fault Coverage

Circuit	*# Test patterns*	*Fault Coverage without Compaction*	*Fault Coverage with Compaction (l = 8)*
p100k	5397	99.56%	99.55%
p141k	5642	98.86%	98.86%
p239k	4778	98.84%	98.83%
p259k	4919	99.10%	99.10%
p267k	5191	99.60%	99.58%
p269k	5164	99.60%	99.59%
p279k	5360	97.89%	97.87%
p286k	6224	98.34%	98.33%
p295k	7916	99.15%	99.14%
p330k	9165	98.95%	98.93%
p378k	664	100.00%	100.00%

In both cases the same pattern set from a commercial ATPG tool was used. It is shown that, despite the response compaction, the proposed method reaches approximately the same fault coverage as the evaluation of the complete test

responses. Table II also shows the size of the test pattern set for each target circuit.

In order to evaluate the achievable diagnostic resolution of the proposed compaction method, stuck-at faults, cross-talk faults, delay faults and wired-and faults were analyzed. A total of 400 faults, 100 faults per fault-model, were randomly and uniformly injected into each circuit. A commercial ATPG tool, like in the experiment above, generated the test patterns. Furthermore, the depth of the fail memory was set to 50. The diagnostic resolution was measured as follows: A fault is said to be correctly diagnosed, if it is the single candidate at the top of the ranked list after the responses in the fail memory have been analyzed. The diagnostic resolution is then defined as the percentage of the faults, which are correctly diagnosed.

Table III first shows the diagnostic resolution without any test response compaction. For every test pattern the full test response is evaluated ("Bypass"). The diagnostic resolution for the method described in section III is listed in Table IV. A total of 32 test patterns are compacted in one test session and $l = 8$ bits are evaluated per session.

TABLE III. DIAGNOSTIC RESOLUTION WITHOUT COMPACTION ("BYPASS")

Circuit	*Stuck*	*Cross*	*Delay*	*Wired-And*
p100k	70%	68%	76%	75%
p141k	83%	61%	79%	67%
p239k	80%	76%	85%	82%
p259k	78%	70%	82%	77%
p267k	79%	63%	70%	69%
p269k	72%	66%	74%	75%
p279k	67%	60%	73%	67%
p286k	76%	56%	67%	68%
p295k	66%	45%	47%	54%
p330k	71%	65%	72%	71%
p378k	87%	91%	95%	93%

TABLE IV. DIAGNOSTIC RESOLUTION WITH THE PROPOSED COMPACTION METHOD (32 TEST PATTERNS PER SESSION, $L = 8$)

Circuit	*Stuck*	*Cross-talk*	*Delay*	*Wired-And*
p100k	83%	67%	78%	76%
p141k	85%	62%	76%	78%
p239k	86%	77%	85%	83%
p259k	79%	69%	83%	77%
p267k	87%	64%	75%	78%
p269k	83%	64%	78%	85%
p279k	79%	56%	68%	73%
p286k	79%	56%	69%	70%
p295k	73%	51%	53%	58%
p330k	71%	66%	73%	73%
p378k	87%	91%	95%	93%

A comparison of Tables III and IV shows that in almost all cases a higher diagnostic resolution is reached. This is due to the constant size of the fail memory. While in the "Bypass" mode every test pattern with a faulty test response produces an entry in the fail memory, the proposed method produces only one entry for each faulty session. Because of this, more information about the defect can be stored in the fail memory and a higher resolution is reachable.

Table V shows the diagnostic resolution for each circuit averaged over all injected faults, both with the proposed compaction method, described in section III, and without any compaction ("Bypass"). The column "Improvement" clearly shows that the diagnostic resolution with the proposed method is in the same range as the diagnostic resolution in "Bypass" mode. In almost all cases the diagnostic resolution improves, and in a few cases the improvement even reaches 5.8%.

TABLE V. AVERAGE DIAGNOSTIC RESOLUTION - COMPARISON

Circuit	*Compaction (32 test patterns per session)*		*„Bypass" average*
	Average	*Improvement*	
p100k	76.0%	+3.8	72.2%
p141k	75.2%	+2.8	72.5%
p239k	82.8%	+2.0	80.8%
p259k	77.0%	+0.2	76.8%
p267k	76.0%	+5.8	70.2%
p269k	77.5%	+5.8	71.8%
p279k	69.0%	+2.2	66.8%
p286k	68.5%	+1.8	66.8%
p295k	58.8%	+5.8	53.0%
p330k	70.8%	+1.0	69.8%
p378k	91.5%	0.0	91.5%

In order to evaluate the hardware costs, the additional memory required for the implementation of the proposed scheme is analyzed: the combined size of the response and fail memories is compared to the memory requirements for the seeds of deterministic test patterns. The method presented in [27] is chosen for this comparison, as it is one of the most efficient pattern encoding schemes found in the literature so far. Table VI summarizes the results.

TABLE VI. HARDWARE OVERHEAD COMPARED TO SEED MEMORY

Circuit	*Input ([27]) [KB]*	*Overhead (%)*
p100k	7.25	5.18%
p141k	36.18	1.06%
p239k	17.97	1.98%
p259k	23.54	1.53%
p267k	47.95	0.77%
p269k	47.44	0.78%
p279k	48.37	0.77%
p286k	63.69	0.63%
p295k	–	–
p330k	76.56	0.64%
p378k	–	–

The second column indicates the required storage for test pattern generation taken from [27] in KB. Column three shows the additional storage requirement when 32 test patterns are compacted in one test session. For almost all circuits the costs for the response and fail memories are negligible compared to those of the seed memory on the input

side. The overhead is, on average, less than 2%. Only for the circuit p100k the memory requirements are significant, about 5%. This results, however, from the well compressible input patterns and not from an insufficient response compaction.

V. Conclusions

For circuits with time redundancy, signature rollback can improve the yield by distinguishing between critical and non- critical faults. This scheme can be combined efficiently with a diagnosis method guaranteeing a high diagnostic resolution. For the diagnosis routine it suffices to use extremely compacted reference data. The storage overhead for the pattern and fail memory is negligible compared to that of the seed memory on the input side for deterministic ATPG.

Acknowledgment

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