Parity Prediction Synthesis for Nano-Electronic Gate Designs

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Abstract

In this paper we investigate the possibility of using commercial synthesis tools to build parity predictors for nano-electronic gates designs. They will be used as redundant resources for robustness improvement for future CMOS technology nodes.

1. Introduction

The CMOS technology scaling allows the realization of more and more complex systems while reducing the production cost and optimizing performances and power consumption as well. Although efficient, each CMOS technology nodes face to reliability problems. However, there is no current technology as effective as CMOS in terms of cost and efficiency. Therefore, it becomes essential to develop methods guarantying a high robustness for future CMOS technology nodes [1].

A high integration density affects the robustness of the circuit during its functioning as well as during its manufacturing. Firstly, it makes the circuit more vulnerable to soft-errors where devices are not permanently damaged. Secondly, it makes the circuit more prone to process variations which induce timing errors. Finally, a high integration density causes a high defect density and thus a lower manufacturing yield.

To increase the robustness of future CMOS circuits and systems, fault tolerant architectures can be one solution. In fact, they are commonly used to tolerate on-line faults, *i.e.* faults that appear during the normal functioning of the system irrespective of their transient or permanent nature [2]. Moreover, it has been shown in [3] that fault tolerant architectures could also be used to tolerate permanent defects and thus improve the reliability.

Fault tolerant architectures use redundancies that are classified in four categories: hardware, software, information and time redundancies [2]. Among these categories, information redundancy, that generally uses detection/correction codes, is the best choice in terms of area overhead (compared to hardware redundancy) and delay penalty (compared to time redundancy).

Parity predictors, used as information redundancy, have already been proposed in [4]. However, the parity predictor synthesis targets only FPGA implementations. In this paper, we investigate the possibility of using commercial synthesis tools to build parity predictors for nano-electronic gate design.

2. Parity prediction synthesis

Parity predictors are obtained by adding the logic structure able to calculate parity check bits from circuit outputs. Then, a commercial synthesis tool is run to generate the gate level description of parity predictors. In this paper, we use only one bit parity code and Hsiao code (with the minimum number of check bits).

Results are presented in Table 1. The area of predictors ("One bit parity code" and "Hsiao code") is presented in percentage of the original circuit ("Overhead / original circuit"), and in percentage of the output independent circuit ("Overhead / OI circuit"). The output independent circuit has the same function as the original circuit, but its outputs have separate logic cones. Such a synthesis approach makes the circuit less vulnerable to errors since only one output can be affected. Output independent circuits are obtained by synthesizing each circuit outputs separately.

Circuit	One bit parity code		Hsiao code	
	Overhead / original circuit	*Overhead / OI circuit*	*Overhead / original circuit*	*Overhead / OI circuit*
c17	71%	60%	na	na
c432	112%	25%	133%	29%
c499	60%	3%	149%	8%
c880	116%	44%	151%	57%
c1355	124%	6%	148%	8%
c1908	114%	12%	143%	15%
c2670	119%	36%	156%	48%
c3540	101%	14%	114%	16%
c6288	103%	7%	109%	7%

Table 1: Synthesis results of parity predictors

In all cases, parity predictors are smaller than the output independent circuit, which are more robust with regard to errors. However, they are usually bigger than original circuit. Therefore, further works on synthesize tools should be carry on in order to provide better parity predictors in term of area.

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