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Variation-Aware Fault Modeling

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Abstract—To achieve a high product quality for nano-scale systems both realistic defect mechanisms and process variations must be taken into account. While existing approaches for variation-aware digital testing either restrict themselves to special classes of defects or assume given probability distributions to model variabilities, the proposed approach combines defect-oriented testing with statistical library characterization. It uses Monte Carlo simulations at electrical level to extract delay distributions of cells in the presence of defects and for the defect-free case. This allows distinguishing the effects of process variations on the cell delay from defect-induced cell delays under process variations.

To provide a suitable interface for test algorithms at higher levels of abstraction the distributions are represented as histograms and stored in a histogram data base (HDB). Thus, the computationally expensive defect analysis needs to be performed only once as a preprocessing step for library characterization, and statistical test algorithms do not require any low level information beyond the HDB. The generation of the HDB is demonstrated for primitive cells in 45nm technology.

***Index Terms*—Defect-oriented testing, parameter variations, delay, analogue fault simulation, histograms**

I. INTRODUCTION

Nano-scale integrated circuits suffer both from high defect densities and from increasing parameter variations [1]. On the one hand, defect-oriented testing tries to overcome the deficiencies of classical fault models by extracting the behavior of library cells in the presence of defects and using this input for automatic test pattern generation (ATPG) at gate level [10]. For cell characterization well-known techniques such as inductive fault analysis [7][25] or inductive contamination analysis [13] can be used.

On the other hand, process variations have led to a paradigm shift in design methods towards what is known as statistical design [27], as well as to the development of novel, variation-tolerant architectures [28]. However, variation-aware testing is particularly challenging. While classical test approaches rely on a clear distinction between the "fault free" and the "faulty" case, parameter variations can change the impact of a defect, and also the parameter variations themselves can lead to an unacceptable behavior [4]. Thus the term "fault coverage" is no longer meaningful. Instead a test must be able to screen out defects for a maximum number of parameter combinations, which is reflected by new test quality metrics as "test robustness" [12] or "process coverage" [32]. As a basis for this new approach to testing both the impact of parameter variations and the impact of defects must be characterized by appropriate statistical models.

Extensive literature is available on modeling process variations [2][8][17][21][30][31]. In the context of testing, a number of publications deal with analog and mixed-signal circuits [5][6][9][14][16][18][20][25]. For digital circuits most approaches either restrict themselves to special classes of defects [10][12] or assume given probability distributions for parameter variations and defect impacts [15][32][33]. The authors of [10] analyze layout based intra-cell faults for an industrial library of digital standard cells and designs to develop and apply a new ATPG. As they only target faults, which do not need any sequential test patterns, analog DC fault simulation is sufficient to generate a set of voltage oriented cell-aware fault detection matrices as input for the ATPG algorithm. Ingelsson et al. [12] focus on resistive bridging faults under process variations.

Liou et al. [15] incorporate statistical information into a static and dynamic timing analysis tool. Their approach calculates delay distributions in the circuit and can be used to select appropriate paths for delay testing. Yilmaz et al. [33] calculate the probabilities that signal transitions will fail to propagate through logic gates within a given time limit. These probabilities are efficiently determined for all the lines in the circuit. Xiong et al. [32] model the variations distributed over the paths in the circuit as random variables for path slacks.

To bridge the gap between low level defect information and the statistical analysis on higher levels of abstraction, the work presented in this paper combines the concepts of defect-oriented testing with statistical library characterization. We present a systematic approach for variation-aware fault model-

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ing for a primitive cell library. For every library cell possible physical defects are represented at the electrical level. To analyze the impact of a defect under process variations, electrical fault simulations with randomly changing circuit parameters are performed. A defect can affect the delay of a library cell or lead to a static fault, which can be viewed as an infinite delay. As a result of this Monte Carlo process for each cell a delay distribution is obtained for each defect and also for the defect-free case. This allows distinguishing between the effects of process variations on cell delays, defect-induced cell delays, and the combinations of both effects.

To provide a suitable interface for fault simulation and test generation tools at higher levels, the distributions are represented by histograms, which are stored in a histogram data base (HDB). The HDB generation step is computationally expensive, but it has to be performed only once as a preprocessing step for library characterization. Statistical test algorithms do not require any lower-level data beyond the histograms in the HDB. This separation is similar to mixed-level fault simulation approaches from the past [22] (these approaches did not incorporate process-variation data). It is also useful for handling the intellectual-property issues in a distributed design, manufacturing and test flow, as the test pattern generation can be done using the HDB only and no sensitive technology data must be given to the entity in charge of preparing the test sets.

The remainder of the paper is organized as follows. Although the focus of this paper is on the generation of the HDB, statistical test algorithms are briefly sketched in the next section to clarify the intended usage of the data in the HDB. Section III outlines the procedures used to generate the HDB and demonstrates the application of the concepts in case of a NAND2 gate. Section IV discusses the obtained results, and finally Section V concludes the paper.

II. Statistical Test Algorithms

The proposed approach for variation-aware fault modeling has been developed within the framework of the project RealTest, which addresses the test of nano-scale systems and aims at integrating statistical modeling into test algorithms, whereby a special focus is put on the test of variation-tolerant architectures. This section briefly summarizes the global view and shows the interfaces between the HDB and the test procedures at higher levels.

As pointed out in the introduction, parameter variations change the behavior of defect-free cells as well as the behavior in the presence of defects, and a clear distinction between fault free and faulty circuits is no longer possible. To reflect the impact of parameter variations, a circuit is called robust for a given range of parameters $P = P_1 \times P_2 \times \ldots \times P_N$, if its functional and delay specifications are fulfilled for all parameter values from that range. For statistical test algorithms the interaction of process variations, defects and delays is of special interest. A defect in a primitive cell or an interconnect may lead to an increased delay or to a static fault (e.g. a stuck-at fault), where the latter can be considered as an instance of an infinite defect-induced delay. The interaction of the defective cell with its surrounding cells and interconnects, which are affected by process variations, may not allow unambiguous decisions whether a given defect is "critical" and should be targeted during test generation. To obtain an appropriate testability assessment on higher levels of abstraction, it is necessary to use probability density functions to describe the behavior of the affected cells.

While classical algorithms are based on the notion of fault coverage as defined in (1), variation-aware testing must be based on new coverage metrics measuring the number of parameter combinations for which the test is effective.

$$FC = \#\,detected\,faults\,/\,\#\,modeled\,faults. \qquad (1)$$

If delay faults with continuous sizes D are considered as in [23] and f_{ds} denotes the density function for defect sizes, Equation (1) becomes

$$FC = \int FC(D) f_{ds}(D)\, dD. \qquad (2)$$

Under process variations, the fault detection depends on the parameter configuration $p = (p_1, p_2, \ldots, p_N) \in P$, and the fault coverage is determined by

$$FC(D) = \int_{p \in P} FC_p(D) f_{pc}(p)\, dp, \qquad (3)$$

where $f_{pc}(p)$ is the probability that the parameter configuration p actually appears in a manufactured circuit instance. In contrast to the conventional fault coverage, i.e. the percentage of faults detected by a test set in a representative circuit with fixed parameter values, Equation (3) describes the percentage of the manufactured instances of the circuit in which the test set detects a given fault. Statistical ATPG must try to maximize this number and generate (compact) test sets identifying the fault in as many valid circuits as possible. This problem is illustrated with the help of Figure 1.

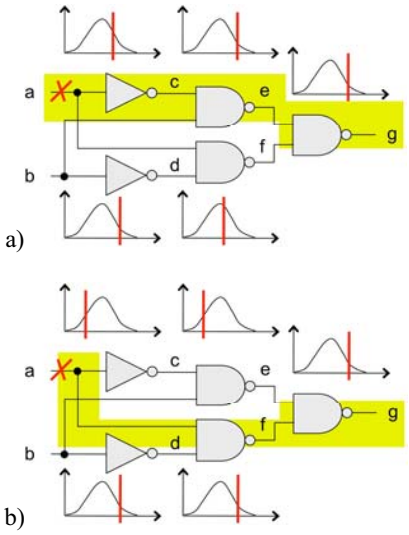

Figure 1. Fault detection under parameter variations.

The circuit in Figure 1 implements an EXOR function using NAND2 gates. To detect a delay fault on input line *a*, conventional delay test generation would try to propagate a transition along the longest path (*a*, *c*, *e*, *g*) in the circuit using the pattern sequence ((*a*,*b*), (*a*',*b*')) = ((0,1), (1,1)). For variation-aware testing the delay distributions of the cells have to be taken into account. For a circuit instance with delays as shown in Figure 1a the path (*a*, *c*, *e*, *g*) is actually the longest path, and the test is a valid test for the delay fault on input line *a*. However, if the actual delays in a circuit instance assume the values as shown in Figure 1b, then the longest path is (*a*, *f*, *g*) and the test is no longer valid. Instead, the test sequence ((0,0), (1,0)) will detect the fault. To maximize the coverage as defined in Equation 3, a test set for this circuit must include both patterns, i.e. T = {((0,1), (1,1)), ((0,0), (1,0))}. This example also clearly shows that the concept of robust delay tests, which detect a delay fault independent of other circuit delays, is of limited use under parameter variations [19].

Figure 2 shows a possible iterative procedure to solve the problem of test generation in this case. Statistical fault simulation determines the parameter range covered by the test patterns generated so far, and a variation-unaware ATPG is invoked with fixed parameter values to cover a further parameter set in the range. This is iterated until an acceptable coverage of the complete range is achieved and can be followed by the compaction of the obtained test set. The data from the histogram data base (HDB) depicted at the top of Figure 2 play a crucial role in these analysis steps.

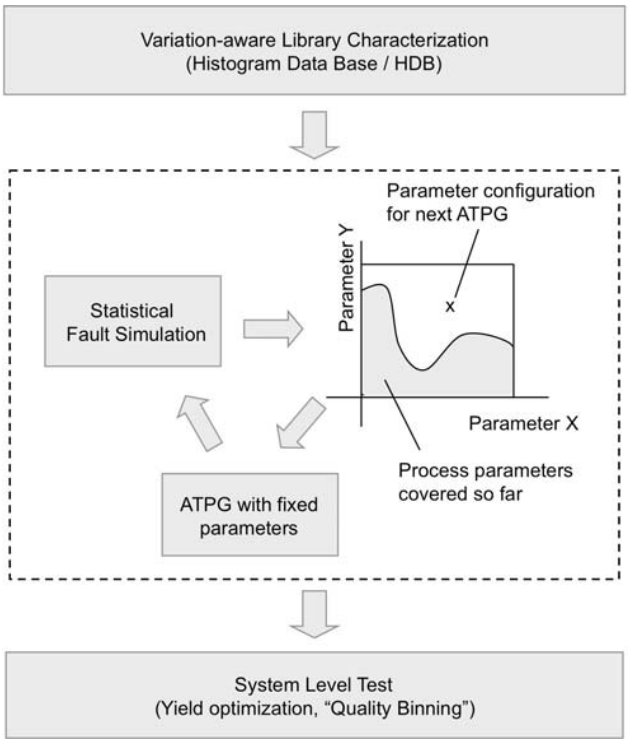

Figure 2. Overview of the statistical test flow.

Based on the knowledge of process-induced variations in the individual circuit components and using high-quality variation-aware test patterns, it is possible to separate the different manufactured instances of a circuit into classes or "bins" according to the frequency or voltage they can handle ("frequency binning" [34] and "voltage binning" [35]), thus maximizing yield. The emerging concept of "quality binning" takes into account the circuit's robustness, i.e. its expected ability to tolerate the effects of ageing or to recover from transient faults. Using the HDB data, it is possible to judge whether the circuit is sufficiently robust, such that its deteriorations will not manifest themselves as observable defects. These system-level approaches based on the HDB data and the outcome of the variation-aware test algorithms are shown at the bottom of Figure 2.

III. HISTOGRAM DATA BASE GENERATION

To describe the generation of the histogram data base, this section first briefly outlines the overall characterization flow and then describes the steps in detail for a NAND2 gate.

A. Characterization Flow

The primitive-cell characterization is done by means of Monte Carlo simulations at the electrical level. For this purpose the analogue fault simulator aFSIM [29] has been extended to allow simulations for varying configurations of process parameters. The simulator takes the following information as inputs:

- a transistor-level netlist,
- a fault list F modeling the effects of realistic physical defects at the electrical level,
- a list of N-tuples $(p_1, p_2, \ldots, p_N) \in P$ representing the parameter configurations to be considered,
- a list of input signals S to be used as test stimuli, and
- an evaluation criterion describing the properties of the circuit to be observed.

The modeled faults include modification, replacement or removal of any circuit element as well as addition of new elements. For the list of input signals, all kinds of analogue and digital sources are allowed. Regarding the evaluation criterion, the cell delay is used in this work, but other options can also be incorporated.

aFSIM automatically computes the fault effects excited by the test stimuli for given parameter configurations. For this purpose, it injects a fault $f \in F$ into the netlist simultaneously with a parameter configuration $(p_1, p_2, \ldots, p_N) \in P$ and hands the resulting circuit to an electrical-level simulator such as SPICE, Spectre, Eldo or TITAN. Here both global and local variations can be considered. A Monte-Carlo fault simulation across the parameter space P consists of $|P|$ repetitions of the same simulation for different parameter configurations. Overall, $|S| \cdot |P| \cdot |F|$ modified netlists are created and simulated to generate the complete HDB. To deal with the high computational complexity of this procedure, the simulations are automatically distributed on a high-performance-computing

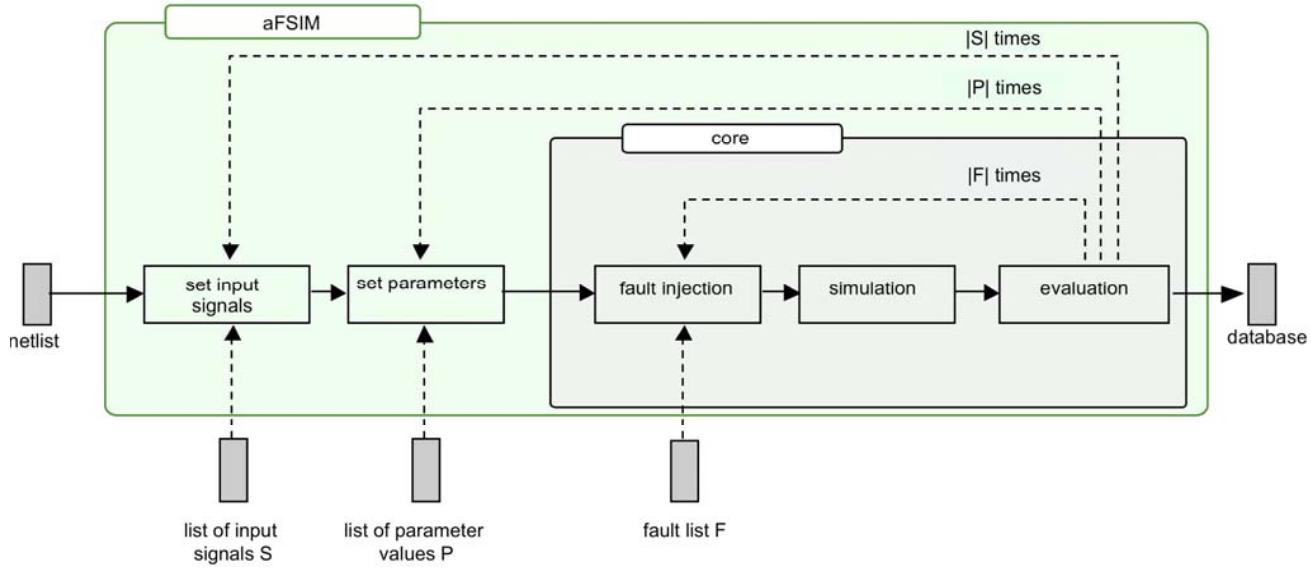

Figure 3. Diagram of the fault simulator aFSIM; simulations are automatically distributed.

(HPC) cluster. The overall architecture of the simulation tool is shown in Figure 3.

B. *Parameter Models, Fault Injection, and Stimuli Generation*

For the characterization flow outlined above the used parameter models, the fault injection procedures, and the stimuli generation are described in more detail using a NAND2 gate as the cell under characterization. Figure 4 shows the circuit model used for electrical fault simulations. The cell itself consists of four transistors and is embedded within a surrounding area for electrical fault simulation. Both inputs of the NAND2 gate are driven by a pair of inverters connected in series. A capacitive load C_L is attached to the cell's output to represent subsequent logic. We used the Nangate 45 nm Open Cell Library (OCL) [3] for all experiments reported in this paper and set $C_L = 0.4\,fF$, a value from OCL statistics [3].

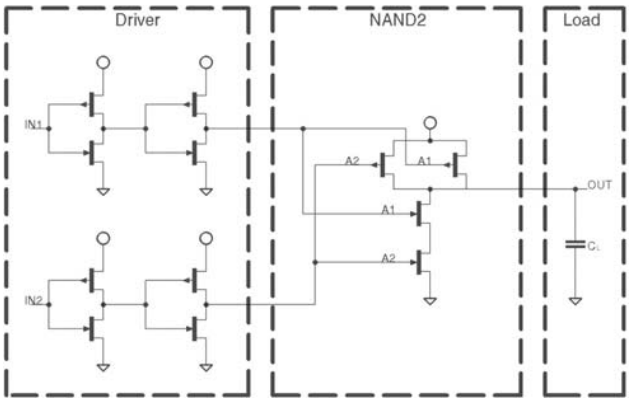

Figure 4. NAND2 gate under characterization with drivers and load.

The information stored in the histogram data base consists of the delays of the cell under characterization assuming different defects and process parameters. Since a NAND2 gate has two inputs, $2^2 \cdot 2^2 = 16$ different test sequences of length 2 (test pairs) can be applied to the gate. At the current status of work, only sequences causing a transition at the output are considered for fault analysis. Table 1 shows the respective test sequences together with the expected digital responses of the defect-free cell.

TABLE I. SIMULATED INPUT SEQUENCES AND CORRESPONDING OUTPUT VALUES FOR THE NAND2 GATE

Test Sequence				Output	
t_n		t_{n+1}		t_n	t_{n+1}
IN1	IN2	IN1	IN2	OUT	OUT
0	0	1	1	1	0
0	1	1	1	1	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	0	1

These six test sequences, modeled as piecewise linear sources with a slew rate of 7.5 ps (a value from the OCL library), are used as input signals for electrical simulations.

The parameter variation model incorporates a total of 14 parameters: channel length L, length reduction parameter L_{INT}, threshold voltage V_{TH0}, bulk effect coefficient K_1, low-field mobility μ_0, junction depth X_J and oxide thickness TOX, for p- and n-channel transistors, respectively. Hence, an instance of the cell under characterization is represented by a 14-tuple specifying the parameters. The variations of the channel length L are modeled based on the data provided by an industrial partner. The parameters are assumed to be uncorrelated as no spe-

cific information about correlations has been available. Furthermore, all considered parameters are assumed to be distributed normally, with mean μ and variance σ derived from the OCL parameters for typical, slow and fast process corners as follows: μ for a parameter is set to this parameter's value in the typical corner; its values in the slow and fast corners are assumed to equal μ – 3σ and μ + 3σ. Figure 5 shows a possible histogram for one parameter and 10,000 samples.

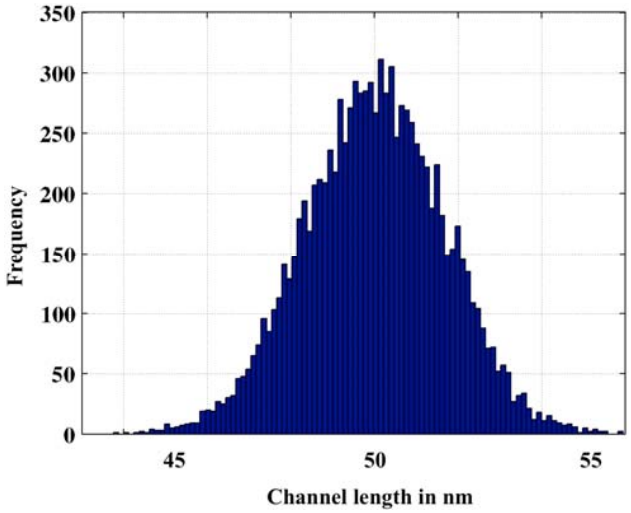

Figure 5. Histogram of the channel length L for μ = 50 nm, 3σ = 5 nm, and 10,000 samples.

At the current status of the project, the fault list contains shorts between wires within the cell and opens of single wires as defects manifestations. No faults are injected in the surrounding logic (the inverter pairs and the capacitive load). The realistic fault list for the NAND2 gate is generated based on the parasitic resistors and capacitances from the extracted netlist. Opens are modeled by replacing a parasitic resistor by a resistor with a high-resistance value. The NAND2 gate has 26 parasitic resistors; since some of them are connected in series and thus result in equivalent faults, only 11 resistors are used as possible open locations. We use 10 different defect resistances between 100 kΩ to 100 MΩ, yielding a total of 110 open defects. Shorts are considered between all terminals of the same transistor and between the gate's inputs. Altogether, there are 13 possible short locations, and 10 different short circuit resistances between 10 Ω to 15 000 Ω. In total, the fault list consists of 110 opens and 130 shorts, i.e., 240 faults. Given six input sequences and 10,000 parameter samples, this implies 6 · 240 · 10,000 = 14,400,000 simulation runs.

IV. Results

The characterization procedure described in Section III has been applied considering time periods of 20 ns for each simulation, where the transition of the input signals begins at 10 ns. The complete characterization takes about 10 days on a HPC-Cluster with 32 nodes. The results are aggregated to histograms and stored in the HDB. To access a histogram, the user must specify a fault and an input sequence; the information which parameter tuples led to which delays are not stored.

Figure 6 shows an open fault in the NAND2 cell under characterization (fault 1), modeled by replacing the parasitic resistor ($R \approx 50\ \Omega$) representing the corresponding wire by a resistor with $R = 500$ kΩ.

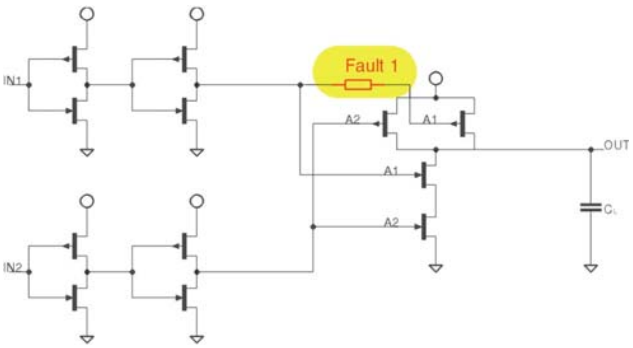

Figure 6. Schematic of the embedded NAND2 gate with injected fault 1.

Figure 7 shows two corresponding HDB entries: the histograms for the defect-free cell and for the cell with fault 1 injected, both assuming the input sequence 00 → 11 (both inputs switch from 0 to 1). Both histograms overlap. This means that some manufactured instances of a circuit with fault 1 in a NAND2 cell may fail the test and others may pass. Furthermore it can be seen that the variation of the delay for fault 1 is greater than the delay of the fault free circuit.

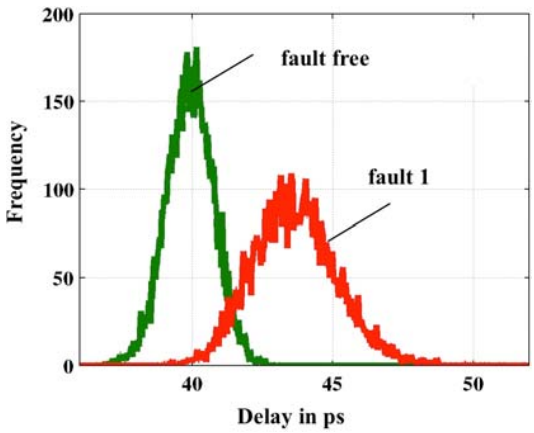

Figure 7. Histograms for the fault free case and for fault 1 obtained for the transition 00 → 11

The histogram for every fault and input sequence can be used as an approximation of the delay distribution across all parameter values. However, there are also faults for which no delay can be determined because no signal transition occurs at the outputs during the observation time. This indicates a static behavior similar to stuck-at faults, which can be interpreted as an infinite delay. For some faults, a finite delay is induced for a number of parameter configurations and an infinite delay for the remaining ones. This is illustrated by fault 2, a 7.5 kΩ short

shown in Figure 8. Its histogram, shown in Figure 9, features a special class, named ∞. It contains parameter tuples for which fault 2 results in static behavior.

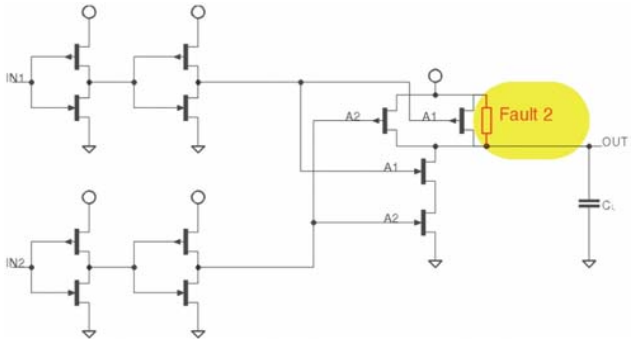

Figure 8. Schematic of the embedded NAND2 gate with injected fault 2.

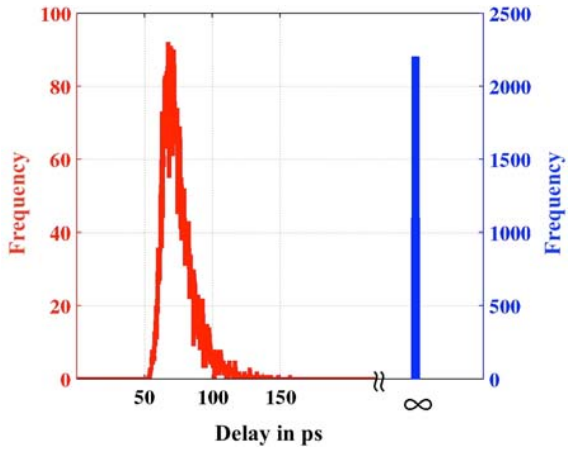

Figure 9. Histograms for fault 2 showing infinite delays.

Out of 14,400,000 simulations for the NAND2 gate a delay could be determined in 67.7% of the cases. For the remaining 32.3% no signal transition occurred during the observation time. The aggregation across the parameter tuples resulted in 1,440 single histograms. 64% of the histograms include no element in class ∞, i.e., they describe only dynamic effects. For 26.7% of the histograms, all elements belong to class ∞; these faults have only static effects. The remaining 9.3% histograms have elements both in class ∞ and in other classes.

The results are summarized in Tables II and III, which show the simulation effort and observed fault effects for the NAND2 gate as well as the corresponding results for two other primitive cells (Inverter, NOR2 gate).

TABLE II. SIMULATION EFFORT FOR SOME PRIMITIVE CELLS

Cell	Input sequences	Injected faults	Simulations
INV	2	150	3,000,000
NAND2	6	240	14,400,000
NOR2	6	240	14,400,000

TABLE III. STATIC VS. DYNAMIC EFFECTS IN HISTOGRAMS

Cell	Effects observed		Classes present in histograms		
	Dynamic	Static	No ∞	Only ∞	Both
INV	55.2%	44.8%	51.0%	37.7%	11.3%
NAND2	67.7%	32.3%	64.0%	26.7%	9.3%
NOR2	62.2%	37.8%	58.8%	32.7%	8.5%

V. CONCLUSIONS

Defect-oriented testing for nano-scale systems must incorporate awareness to massive process variations. The proposed approach combines defect-based fault modeling with statistical library characterization. It is based on an enhanced version of the analogue fault simulator aFSIM, which incorporates transistor-level fault modeling and parameter variations. The obtained delay distributions are aggregated to histograms and stored in a histogram data base (HDB). The HDB can be flexibly accessed and efficiently used by algorithms such as delay fault simulation or ATPG at logic level. This allows to clearly separate the low-level electrical information from test algorithms operating at the higher abstraction levels.

HDB generation has been demonstrated in detail for a NAND2 gate, and it has also been applied to an inverter cell and a NOR2 gate using the data for primitive cells in Nangate 45 nm OCL. The obtained information accurately distinguishes between effects of process induced parameter variations and the effects of manufacturing defects. Furthermore, it has been shown that the same manufacturing defect can lead to a delay fault or to static fault (infinite delay) depending on the parameter configuration.

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