Open Seminar RA, Winter 2020 in Reichenau

January 14th-16th

Attendees: WU, ES, AA, NL, PNH, PW, MN

- **Tuesday, January 14th, 2020**

  08:15: RAMIs meet at Stuttgart Hbf
  08:29: Train from Stuttgart Hbf to Reichenau(Baden).

  12:15-13:00: Lunch

  14:00-15:30: **Ahmed Atteya**:
  "Fault Simulation of Reconfigurable Scan Networks"
  Reconfigurable scan networks (RSN) offer flexible access to on-chip instrumentation. To ensure dependable access to on-chip instruments,the RSN itself must be thoroughly tested and validated. Accurate simulation is required to validate low level effects such as setup and hold time validations, delay faults and glitches. In this talk new ideas about accelerating the fault simulation for RSNs will be presented and the next steps will be discussed.

  15:45-17:15: **Natalia Lylina**:
  "On Dependable Partitioning of Reconfigurable Scan Networks"
  Numerous instruments, such as aging monitors, logic and memory BISTs, are used nowadays to ensure the reliability of safety-critical devices throughout the entire life-cycle. Reconfigurable Scan Networks (RSNs) can be used to provide an efficient and flexible access to the instruments. However, improper RSN integration introduces new data paths to the initial circuit. Such additional paths must be considered as a security violation, since an attacker can them to gain an unauthorized access to the functional circuit.
  In this paper we propose a method to optimally repair the RSN using integer linear programming algorithms. A minimal number of structural changes is applied to the RSN structure to make it compliant to the initial security requirements and preserve the testability of all the scan segments in the RSN.

  18:00-19:00: Dinner

- **Wednesday, January 15th, 2020**

07:30: Breakfast

09:00-10:30: **Marzieh Nazari**

"Online periodic BIST for SDF"

Small Delay Faults (SDF) introduce reliability threats throughout the life cycle of a chip. Since SDFs on short paths may not affect the functionality of the chip, they may not be detectable during manufacturing test. However, they can result in functional failures and early life failures over time. Therefore, they must be screened out during manufacturing test. Furthermore, their evolution in the field must be proactively monitored by periodic tests before actual failures occur. Faster-than-at-speed test (FAST) can detect such hidden delay faults (HDFs), but so far FAST has mainly been restricted to manufacturing tests. Hence, a fully autonomous built-in self-test approach, which can support in-field periodic testing of SDFs in transition level, can be an appropriate solution. During the presentation, I will explain each of these terminologies as well as some related works along with their challenges in detail. Besides, I will propose some ideas to overcome the limitations of the online test of SDFs.

10:45-12:15: **Paria Najafi Haghi**

"Variation-Aware Marginal Defect classification at Cell-Level"

The high rate of ELF, demonstrates the necessity of considering marginal defects as a source of ELF-related faults. SDFs indicate marginal defects in a circuit, which has a comparable size which is comparable in size with the delay that is caused by process variations. However these two types of delays should be distinguished, since unlike process variations, marginal defects are threat to reliability. In this work simulated parametric behavior under varying power supply voltage of defect and fault-free instances are used to train statistical learning schemes as classifiers. 3 different ML algorithms are trained with the data set of fault-free and defect parametric behaviors. Trained MLs provide classifiers for various defect-type for each cell in FinFET OCL. Parametric behavior of a new cell goes through all the classifiers to be checked for marginal defect. The classification efficiency are calculated by quality metrics using two different validation methods. 10-set cross validation shows the accuracy of the classification can be as high as 100%. However overlap-based validation as the worst case scenario shows more that 90% for most of the cases. In the NAND cell case study in this work, kNN algorithm classifies with 0.95% accuracy for the overlap-based validation and up to 100% precision in both validation methods. In addition, it has the minimum memory usage and computation time. This makes the kNN algorithm an appropriate classifier for this cell-type. A comprehensive classifier for each cells in OCL is once trained and is ready to be used for further classification of new cells. By distinguishing marginal defects from process variation, the reliability of devices will be increased while the production yield in maintained high.

12:15-13:00: Lunch

18:00-19:00: Dinner

- **Thursday, January 16th, 2020**

07:30: Breakfast

09:00-10:30: **Chih-Hao Wang**
"A Cost-Effective Concurrent Error Detection Method Based on Logic Implications"
As the high demands in reliability for mission-critical applications such as automotive eletronics, aviations, etc., concurrent error detection (CED) techniques provide solutions to monitor the correctness of the computational results. In recent years, logic implications have been shown to have good potential to implement a CED scheme. This work presents a complete solution to implement a cost-effective implication-based CED scheme. By strategically combining with other CED schemes, our approach simultaneouly improves the probability of detecting errors as well as the diagnosability of the circuit under test. In order to reduce the hardware cost, an implication reduction method and a signal collapsing technique are presented. Except the conventional stuck-at and transition delay fault models, this work employs the small delay fault model to evaluate the effectiveness as well. A novel solution is presented to further improve the error detectability caused by the small delay faults. This work also presents an application based on the notion of the logic implication to test reconfigurable scan networks (RSNs) during online operations.

10:45-12:15: **Eric Schneider** (Rehearsal for DATE):
"GPU-accelerated Time Simulation of Systems with Adaptive Voltage and Frequency Scaling"
Timing validation of systems with adaptive voltage-and frequency scaling (AVFS) requires an accurate timing model under multiple operating points. Simulating such a model at gate level is extremely time-consuming, and the state-of-the-art compromises both accuracy and compute efficiency.
This paper presents a method for dynamic gate delay modeling on graphics processing unit (GPU) accelerators which is based on polynomial approximation with offline statistical learning using regression analysis. It provides glitch-accurate switching activity information for gates and designs under varying supply voltages with negligible memory and performance impact. Parallelism from the evaluation of operating conditions, gates and stimuli is exploited simultaneously to utilize the high arithmetic computing throughput of GPUs. This way, large-scale design space exploration of AVFS-based systems is enabled. Experimental results demonstrate the efficiency and accuracy of the presented approach showing speedups of three orders of magnitude over conventional time simulation that supports static delays only.

12:15-13:00: Lunch
14:00: Departure from Reichenau after lunch.