Towards Variation-Aware Test Methods

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Proceedings of the 16th IEEE European Test Symposium (ETS'11) Trondheim, Norway, 23-27 May 2011

doi: http://dx.doi.org/10.1109/ETS.2011.51

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Preprint

Towards Variation-Aware Test Methods

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Abstract— Nanoelectronic circuits are increasingly affected by massive statistical process variations, leading to a paradigm shift in both design and test area. In circuit and system design, a broad class of methods for robustness like statistical design and self calibration has emerged and is increasingly used by the industry. The test community's answer to the massive-variation challenge is currently adaptive test. The test stimuli are modified on the fly (during test application) based on the circuit responses observed. The collected circuit outputs undergo statistical post-processing to facilitate pass/fail classification.

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***Index Terms*—Parameter variations, Adaptive test, Delay test**

I. INTRODUCTION

Massive statistical process parameter variations are a grand challenge in design and test of nanoscale integrated circuits [1]. These process variations occur due to limited accuracy of various manufacturing steps. For example, subwavelength lithography in combination with optical proximity correction approaches causes line-edge roughness, i.e., slightly different shapes of objects on different manufactured circuits. They affect parasitic capacitances between interconnects and thus the signal-propagation delays. Moreover, atomic-scale concentrations of dopants in active regions may be extremely hard to control. Even a few missing or extra dopant atoms can significantly change a transistor's threshold and therefore it's switching delay or the current it consumes. While process variations have historically been considered in the context of analog circuits, they affect digital circuits in state-of-the-art nanoscale manufacturing technologies. A variety of design and analysis methods have been developed to cope with variations, and all major electronic design automation software vendors offer commercial products with such capabilities.

However, testing circuits affected by massive process variations is a challenge of its own [4]. Classical test methods which do not consider process variations turn out to be inadequate for such circuit populations. On the one hand, they may not be sufficiently effective, i.e. they may miss defects in some of the circuits that have specific parameter combinations. On the other hand, they may be inefficient, that is, require an unreasonable amount of resources. For example, *n*-detection (testing the same fault by *n* different test patterns) [34] tends to increase the test quality, yet it also leads to a significant increase of test data volume and test application time.

Most researchers working on what we call *variation-aware test,* followed the basic principle of defect-based test [43]. The variation-aware test methods attempt to model the physical mechanism of the failure and its interaction with process variations. These models must be as accurate (i.e. as close to the physical reality) as possible. Tests to be applied are derived based on these models, and are typically evaluated by some variation-aware test-quality metric. For example, one could attempt to cover small-delay faults of various sizes under the assumption that delays of all the logic gates in the circuit are statistically distributed rather than fixed. In theory, this allows very systematic, pinpointed test generation for the relevant defects under many possible parameter combinations. In practice, the accuracy of the models employed is bounded by two factors: insufficient understanding of physics behind the failure mechanisms, and computational feasibility of algorithms based on these models. Furthermore, even if simplified models are employed, the complexity of variation-aware test generation is considerably larger than for simple traditional fault models such as stuck-at or transition faults. Variation-aware test generation also requires low-level electrical data to model the circuit, the variations, and the defects, which are not required for traditional testing.

A radically different approach employed to test populations of circuits having process variations is known under the heading *adaptive test*. During adaptive test, the test conditions are modified based on the test results observed so far. Adaptive test methods generate knowledge on which tests have been effective in capturing defects in the past and make decisions which tests should be applied or skipped in the future such as to meet

This work has been performed within the framework of the project RealTest sponsored by the German National Science Foundation (DFG).

quality demands while not wasting resources. The purpose of adaptive test is not necessarily to obtain detailed understanding of what exactly went wrong in the failing circuit. Instead, its purpose is to identify failing parts with a sufficient confidence while fulfilling the economic constraints. One representative adaptive test technique is neighborship analysis: a die is subject to more intensive testing if its neighboring die had defects.

In this paper, we give an overview over current and future developments of different types of variation-aware testing, including adaptive test methods used in the industry. We further discuss how detailed information collected by variation-aware test method could be leveraged to facilitate adaptive test and diagnosis.

II. Variation-Aware Test

As pointed out above, many variation-aware test approaches aim at pinpointedly targeting defects in a circuit affected by process variations. Consequently, these variation-aware test methods require an electrical model of the defect-free circuit elements under parameter variations as well as a model of the defect. There is extensive literature on modeling process variations in the absence of a defect as well as on modeling defects in a circuit without process variations. We first provide some information on these modeling approaches before describing their combination in variation-aware test. In the context of testing, one relevant value affected by process variations is circuit timing. For this reason, many of the methods covered are targeted toward delay faults.

A. *Variation-aware design*

There are several books on physical modeling of process variations, including [41], as well as recent tutorials on the topic such as [18]. Process variations data can be obtained by extracting a large amount of process data [44]. An approach to statistically model the performance of gates and interconnects is found in [3] [26]. Variation effects distributed over entire paths are modeled in [28]. Correlations are accounted for in, e.g., [39].

A variety of methods has been developed to cope with process variations on different levels of the design. Early developments are known under the heading "statistical design" [12]. Problems for which specific variation-aware techniques have been proposed include transistor sizing [7], yield optimization [5] and voltage binning [46]. Insertion of circuit elements to compensate for variations of propagation delay has been considered for delays in clock distribution networks [33] and in arbitrary logic gates [44]. Self-calibration techniques such as adaptive body bias and adaptive supply voltage are further methods at the designer's disposal [6]. There are also several techniques on higher abstraction levels including Razor [14] and its variants [25] which aim at achieving energy-performance optimum under process variations. A further high-level variation-aware design approach is reported in [42]. All these statistical design methods tend to prevent or conceal corner-case situations when the circuit operates very close to or beyond its specifications. Since the task of test is to expose these very situations, a circuit designed using statistical methods poses special challenges for testing.

B. *Defect-based test*

The term defect-based test summarizes a variety of test methods based on accurate electrical modeling of defects in a circuit. An early systematic defect-based approach was *inductive fault analysis* [15] [37] followed by *inductive contamination analysis* [24]. Specific defect-based fault models considered in the last few years are resistive bridges [13] and interconnect opens [20]. A comprehensive summary of recent developments is found in [43]. An example industrial application of defect-based test is reported in [19]. Of specific importance in the context of process variations are defect-based approaches to modeling delay defects, including [8].

C. *Variation-aware fault coverage metrics*

The first difficulty in variation-aware test is to define when a fault is actually "detected" by a test pattern or a test set, and, consequently, the "fault coverage" of such a test set. Consider the circuit in Fig. 1. The delays of the gates are described by Gaussian distributions shown, and the red vertical lines indicate, for two manufactured instances of the same circuit, actual delays of the gates. It is obvious that testing of the small-delay fault on line *a* must sensitize different paths for these two instances. The test pair 01/11 may detect the fault in the instance in Fig. 1a while missing it in the instance in Fig. 1b, while the opposite is true for pair 00/10. Hence, a specific understanding of "detection" is required.

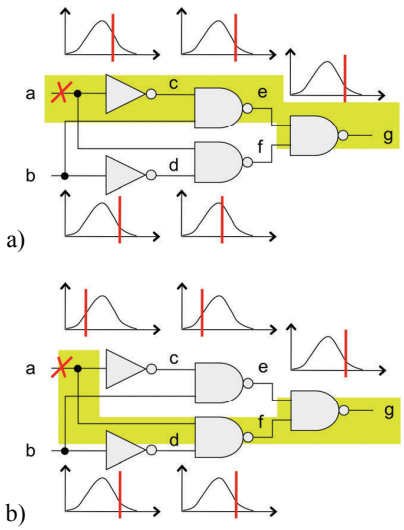

Figure 1. Fault detection under parameter variations [21].

The fault coverage is traditionally defined as

$$FC = \#\,detected\,faults\,/\,\#\,modeled\,faults. \qquad (1)$$

For delay faults with continuous sizes D, fault coverage is defined as follows [35]:

$$FC = \int FC(D) f_{ds}(D)\, dD, \quad (2)$$

where f_{ds} denotes the density function for defect sizes. The following approach to model process variations is taken in [21]. Let $p = (p_1, p_2, \ldots, p_N)$ be a *parameter configuration*, i.e., a list of actual values of every process or technology parameter affected by variations. Let P be the set of all possible parameter configurations. Hence, each manufactured instance of the circuit corresponds to one $p \in P$. Then, the fault coverage for a small-delay fault with a given size D is given by

$$FC(D) = \int_{p \in P} FC_p(D) f_{pc}(p)\, dp. \quad (3)$$

Here, $f_{pc}(p)$ is the probability of parameter configuration p showing up in a manufactured circuit instance. On the one hand, statistical ATPG may try to maximize this number and generate (compact) test sets identifying the fault in as many valid circuits as possible. On the other hand, this means that some of the patterns in the test set may be ineffective for any fault in some of the circuits. For this reason, it is, in general, optimal to apply subsets of the complete variation-aware test set to each manufactured circuit instance. This is exactly the philosophy of adaptive test introduced before.

D. Representative variation-aware test algorithms

In the following, we present several simulation and test generation algorithms which explicitly target process variations. Liou et al. [27] target delay faults in circuits with statistically distributed delays of each logic gate. They also considered specific noise mechanisms and their implications on gate delays. One outcome of their method is the list of paths which should be targeted by delay fault ATPG for a comprehensive coverage under process variations.

Ingelsson et al. [22] extend earlier parametric resistive-fault models to incorporate effects of process variations. They employ a metric which they call "process coverage".

Yilmaz et al. [45] focus on delay faults under process variations. They consider a propagation time budget for a gate and calculate the probabilities that signal transitions will fail to propagate within this budget. An efficient algorithm to calculate these probabilities for all locations in the circuit is proposed.

Xiong et al. [44] introduce a statistical model which maps the variations distributed over the paths in the circuit to random variables that represent path slacks.

Hopsch et al. [21] propose a systematic approach to use process-variation data in high-level test algorithms. They consider delay implications of resistive defects in primitive cells. For each considered defect, they perform a Monte-Carlo simulation which yields the histogram of delays observed for the cell with this fault under 10,000 different parameter configurations. All such histograms are stored in a data structure called *histogram data base* (HDB).

Fig. 2 shows one suggestion how to use the data from the HDB for higher-level test algorithms. The framework maintains a representation of parameter configurations covered by the test patterns generated so far. For each new pattern, it is calculated which parameter configurations (or ranges thereof) it covers, i.e., for which possible manufactured instances it will detect the fault. This calculation is performed by statistical fault simulation. Then, a parameter configuration which has not yet been covered is identified and ATPG is run to create a pattern for this configuration. This establishes a loop which terminates once the coverage target has been reached. Details on how the information gathered during iterations is useful for emerging system-level yield optimizations and "quality binning" can be found in [21].

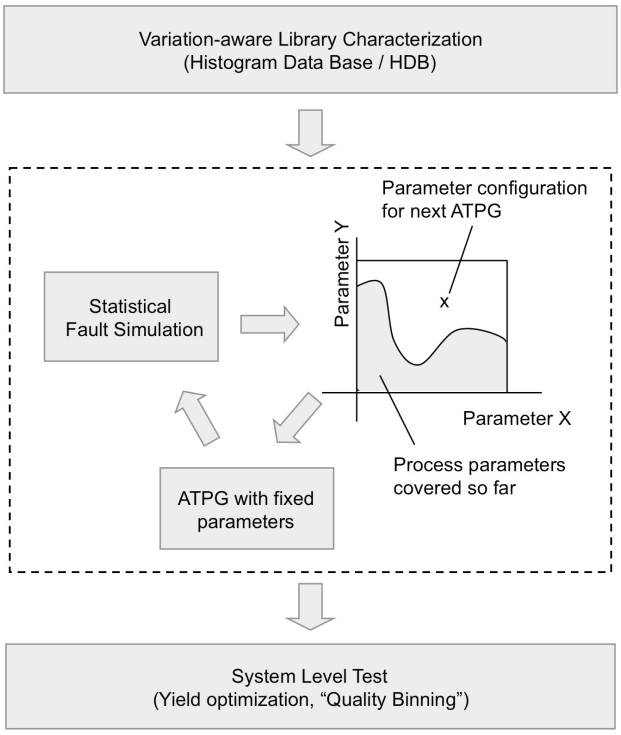

Figure 2. Statistical test flow [21].

III. ADAPTIVE TEST

As described in ITRS 2009 [1], *adaptive test* is a broad term used to describe methods that change test conditions, test flow, test content and test limits based on manufacturing test data and statistical data analysis. The granularity of the changes is very broad and can potentially be applied at the sub-die level. In this case, different blocks in a chip would have tests adapted from the responses of other blocks. At the other extreme, post-test statistical analysis can be used to optimize testing of future products.

Included in the definition is feed-forward from inline test and early test steps to later test steps and feed-back data from post-test statistical analysis of later test steps that is used to optimize earlier steps. For example, excessive package fallout could trigger more rigorous wafer test. More generally, off-line analysis would be used to optimize test flows, test content and measurement routines. Off-line analysis combines data from many sources including historic data collected, test capacity,

required turn-around times, DPM requirements, expected yields and parametrics. Conversely, larger than usual wafer fallout could trigger more extensive burn-in. Feed-forward can also be used within a test step, an example being Madge et al. [29] where a reduced vector set is used to obtain an estimate of the minimum operating voltage ($minV_{DD}$) and this is fed forward to the full vector set to be used in pass/fail criteria.

The above are examples of the more general concept of performing data analysis that can be used to adjust test limits and content during production testing on-the-fly. The analysis can occur either in real-time (in parallel with testing), near-time (at the end of sample testing and at the end of wafer test and lot test) and off-line. Compared to traditional test, the emphasis is on dramatically shortening the cycle time of any modifications done and to minimize direct input by product and test engineering staff.

Central to such an adaptive system is a shared database and off-line analysis system. The database is built up not only from information acquired during test, but also from many other inputs, any or all of which could affect how testing is done. For example, an urgent business need for parts with a speed bin lower than the maximum might trigger rebinning to change otherwise high speed bin parts to lower speed bins. Fab data indicating a fast or slow lot may change criteria under which some speed tests are dropped or added.

Each test step can have real-time and near-time (e.g., end of wafer) analysis capability and can access information from this database. Real-time analysis capability could be during the test of an individual die, between consecutive dies or within a very short time window (e.g., within 5 seconds). Such an analysis is needed to allow dynamic changes in test content and flow at the die level. An important constraint is that the analysis must not significantly slow down testing.

A general system would also enable full feed-forward and feed-backward of data and analysis results from any test step to any other one.

A. Outlier Screens and Data Driven Test

Adaptive test is based on using data obtained from one part of the test process to modify some other part. Variants of adaptive test differ regarding what value is measured and what test procedure is modified. The basic approach involves defining an algorithm which sets test limits or test content/flow. During test execution, real-time (and possibly historical) DUT response data is used as input to the limit setting or test content/flow setting algorithms. A distinguishing feature is that the algorithms are statically defined, and although the outputs vary from die to die, the method of computing the output does not.

The two most common reported applications are for test time reduction and for improved screening quality. Many early implementations were referred to as "outlier screens" and changed the basis of testing from "is the part good" to "is the part different", resulting in parts which pass all tests as being within specification, but rejected because they lie outside the expected distribution of one or more parametric measurements. The first paper to use the term "adaptive test" was Singh and Krishna [38], where data obtained from neighboring die is used to predict the yield of the device under test. Using this prediction, the test length (or, equivalently, fault coverage) is adjusted to obtain the desired defect level, resulting in improved test times or improved quality for the same test time.

Other early adaptive methods were concerned with I_{DDQ} test, when it became evident that a fixed threshold approach was ineffective, given the large variations seen in leakage current from die to die [31]. Rather than having a fixed limit, a procedure or algorithm is defined which sets test limits. Parameters for the algorithm are obtained during characterization and are then fixed for all die. During test execution, real-time DUT response data collected by the tester is used as input to the limit setting algorithm, which calculates the appropriate limit on an individual die basis. Examples for Iddq are the ratio of maximum to minimum current ("current ratios" [31]), significant steps in the sorted currents ("current signatures", [16]) and changes in one vector to the next ("delta- I_{DDQ}" [32]). Similar concepts were applied to $MinV_{DD}$ testing, where a predicted value of $MinV_{DD}$ was obtained from measurements of neighboring die and this value became the limit for the die under test [11].

Similar approaches can be used in *delay test,* which is particularly susceptible to significant variability. Unlike I_{DDQ} or $MinV_{DD}$, delay is typically not measured directly since firstly it would take too much test time to do so during production and secondly, due to on-chip variation there is no one path that represents the "speed" of the die. Instead, indirect measurements are made, such as ring oscillator frequencies (several ring oscillators can be placed on each die, as in [17]) or maximum frequency of operation, F_{max}.

F_{max} and I_{DDQ} are well-known to correlate and have been used as a two-parameter test with adaptive limits [23]). F_{max} can be used in other ways, however. Daasch et al. [10] used neighboring die to predict the expected value of I_{DDQ}, thereby adapting the limit of the die under test. F_{max} could be used the same way, with values from a neighborhood used to determine an expected value, and reject the die if the measured value is outside some allowable range, even if it is within spec. Such an approach relies on *variance reduction*. That is, the variance of the distribution of the residuals of measured versus predicted F_{max} is less than the variance in F_{max} itself. Variance reduction is a powerful method to reduce yield loss and improve quality, as illustrated in Fig. 3, which shows the distributions for defect free and defective parts for some parameter, together with the test limit for that parameter. The overlap contributes to both yield loss and test escapes. Test escapes arise when parts which are actually defective lie on that part of the curve which is less than the test limit. Conversely, good parts which lie on the part of their respective curve which is higher than the test limit get rejected. Fig. 4 shows equivalent distributions for a derived test limit, for example, the residual from a predicted value. Here the overlap is much less, meaning lower yield loss and fewer escapes. Derived parameters therefore serve to distinguish a defective part which would otherwise appear to be normal.

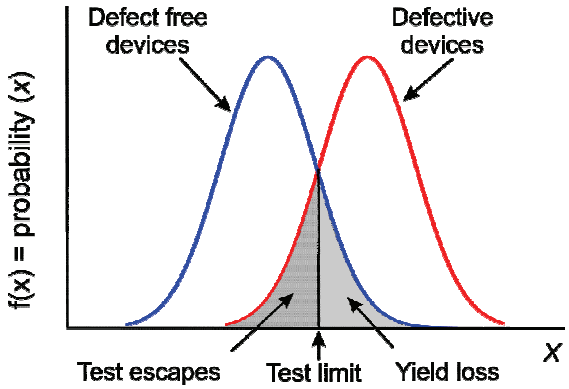

Figure 3. Distribution of original parameter x

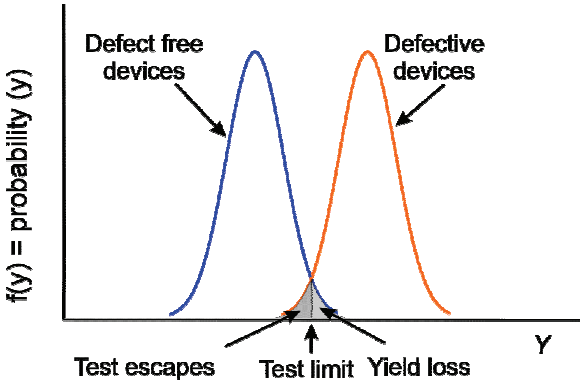

Figure 4. Distribution of derived parameter y

Small delay defect testing is another area which can be improved with an adaptive approach. Any given delay defect size on any given path will have a different effect depending on the speed of the path on the die under test. Although it would be extremely difficult to predict individual path speeds, it is clear that faster dies are going to be more susceptible. This opens the possibility of using speed data such as ring oscillator frequency to determine the rigor of small delay testing. Slow die would be adequately screened with a larger cutoff in the delay size to be tested.

B. *Benefits and Challenges of Adaptive Test*

A more extensive discussion of this topic is found in [30]. Briefly, the results of applying adaptive test are lower test costs (through test time and yield loss gains), quality and reliability (through improved screening), improved yield learning (through the availability of data which is of necessity collected for an adaptive approach), and test floor efficiency improvements.

In the uses of adaptive test seen so far, the models have been fixed. For more advanced implementations, methods need to be developed where the models themselves are dynamically adjusted based on DUT responses. Even for present approaches, better peripheral coverage metrics are needed to understand the quality impact of dropped or modified tests. This can be done using empirical data, but is not scientific.

Cost-conscious chips are frequently tested in a multi-site configuration to save test cost [40]. This results in the touchdown time being determined by the site which takes the longest, which is typically the entire test since at least one of the sites is expected to pass all tests. Adjusting content based on test time will therefore have little or no benefit unless a sophisticated method is used where different sites have a different mix of tests, each of which taking less time than a complete flow. For such an approach, test equipment is required with separate controllers for each site. Benefits could still be obtained by having a short flow on predicted high yield groups of sites and a long flow on others, but this requires expanding the region of prediction from a single die to many. Since it is not uncommon to have 8 or 16 sites in a touchdown, considerable variation could be expected across the sites, imposing challenges in implementing an effective adaptive strategy.

IV. Emerging Concept: Variation-Aware Adaptive Test

A major reason for the effectiveness of adaptive test is the existence of correlations in process parameters between dies from the same lot. In the following, we indicate how considering additional low-level information explicitly can further increase the accuracy and thus the efficiency of adaptive test.

Today, test patterns or, for delay testing, test sequences are typically annotated with diagnostic information. For each test t_i, the list of faults detected by t_i can be obtained. Using statistical fault simulation mentioned above, it is possible to enrich diagnostic information with process parameter data. For each t_i and each fault detected by t_i, the process parameters for which the fault is detected can be provided. We illustrate one possible use of such information by an example.

Assume that the only modeled parameters affected by variations are gate delays. For a circuit with N gates G_1 through G_N, a manufactured instance of the circuit is determined by the delays δ_1 through δ_N. Let $\mathbf{\Delta}$ denote the *parameter space,* i.e., $\mathbf{\Delta}$ includes all possible tuples $(\delta_1, \ldots, \delta_N)$. Assume that this parameter set is divided into three parameter sub-spaces Δ_1, Δ_2 and Δ_3, with $\Delta_1 \cup \Delta_2 \cup \Delta_3 = \mathbf{\Delta}$. For instance, a circuit with parameters from Δ_1, Δ_2 and Δ_3 may have low, medium, or high speed, respectively. However, also other definitions of sub-spaces are possible. Each test is annotated with combinations of faults from the fault list and parameter sub-spaces for which the fault is detected. Consider the following example with five test tests and three faults:

$t_1 \rightarrow f_1/(\Delta_2, \Delta_3)$
$t_2 \rightarrow f_1/\Delta_2, f_2/\Delta_2$
$t_3 \rightarrow f_3/\Delta_1$
$t_4 \rightarrow f_1/(\Delta_1, \Delta_2)$
$t_5 \rightarrow f_2/\Delta_1, f_3/\Delta_1$

(This means that t_1 detects fault f_1 in circuits with parameter combinations $(\delta_1, \ldots, \delta_N) \in \Delta_2 \cup \Delta_3$, t_2 detects f_2 in circuits with parameter combinations $(\delta_1, \ldots, \delta_N) \in \Delta_2$, and so on.) Suppose that a circuit fails for t_3 and t_5. Conventional adaptive test will assume that other circuits are also likely to fail for these inputs. In order to identify failing circuits more quickly, the test pattern set may be re-ordered to $(t_3, t_5, t_1, t_2, t_4)$. On the

other hand, variation-aware adaptive test set would first try to analyze *why* the circuit failed for t_3 and t_5. A straightforward explanation for this failing pattern is that the failing circuit's parameters are from parameter sub-space Δ_1.

Assuming correlations between dies from the same lot, the next circuits under test will probably also have parameters from that sub-space. The above-mentioned ordering (t_3, t_5, t_1, t_2, t_4) would detect f_3 in such a circuit by the first applied pattern (t_3), and it would detect f_2 by the second applied pattern (t_5). However, a circuit from sub-space Δ_1 having fault f_1 would only be identified by the last test t_4. Hence, it would be useful to move t_4 closer to the beginning of the test set.

One further optimization can be derived from comparing the faults and the sub-spaces covered by t_3 and t_5. It can be seen that all the (modeled) fault/sub-space combinations detected by t_3 are also detected by t_5. Hence, t_3 does not appear to be essential. t_3 can only identify a failing circuit missed by t_5 in the case of an unmodeled defect, which is unlikely although not completely impossible. Consequently, it makes sense to move t_3 to the end of the sequence. A variation-aware adaptive test approach may thus result in sequence (t_5, t_4, t_1, t_2, t_3). Figure 5 illustrates the procedure.

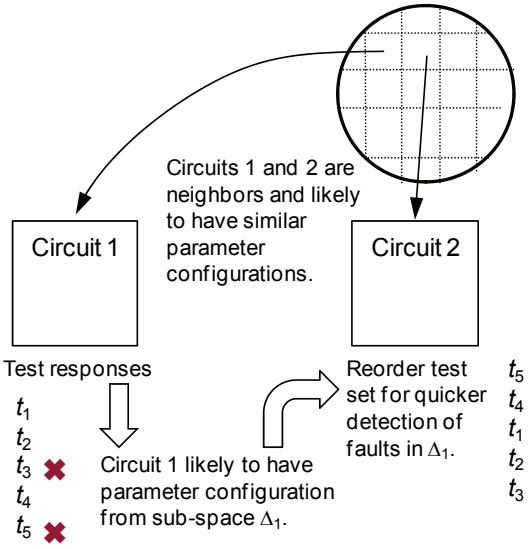

Figure 5. Variation-aware adaptive test re-ordering.

Another possible use of the variation-aware diagnostic information is the identification of potential coverage gaps. In the example above, two out of three faults are not detected for sub-space Δ_3. It may be worth considering generating additional tests targeting these faults explicitly, and apply or skip these tests depending on information previously collected. To perform variation-aware test generation, state-of-the-art multi-constrained SAT-based ATPG tools [8] can be employed in a manner indicated in Fig. 2. Such tools can also identify faults that are undetectable under specific parameter configurations and therefore need not be tested.

Variation-aware adaptive test re-ordering requires a higher amount of diagnostic data computed before test application than the standard approaches. This information may be complemented and enhanced based on responses observed during test application. For example, consider again a circuit passing for t_3 but failing for t_5. As stated above, this situation can be explained by an unmodeled defect and should not occur often. However, if many circuits pass for t_3 but fail for t_5 during actual test application, this gives a hint that the underlying model is inadequate and should be refined. For example, the division of $\boldsymbol{\Delta}$ into $\Delta_1 \cup \Delta_2 \cup \Delta_3$ could be too coarse-grained and a larger number of smaller sub-spaces could be required. The decision strategies in the context of variation-aware adaptive test are a promising direction for future research.

V. CONCLUSIONS

Statistical process variation can no longer be ignored during test. A variety of (mostly academic) variation-aware test methods based on accurate low-level modeling of defects and variations exists. We reviewed several representative techniques, focusing on delay implications of process variations. The industry currently tends to employ simpler adaptive test approaches. We provided a brief overview of adaptive test methods and summarized challenges that remain to be solved. Furthermore, we devised one possible way to incorporate accurate variation-aware diagnostic data, represented by parameter space partitions, into adaptive test schemes. Such combined test strategies can be feasible economically while providing sufficient defect coverage at the same time.

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