A Diagnosis Algorithm for Extreme Space Compaction

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***Abstract*— During volume testing, test application time, test data volume and high performance automatic test equipment (ATE) are the major cost factors. Embedded testing including built-in self-test (BIST) and multi-site testing are quite effective cost reduction techniques which may make diagnosis more complex. This paper presents a test response compaction scheme and a corresponding diagnosis algorithm which are especially suited for BIST and multi-site testing. The experimental results on industrial designs show, that test time and response data volume reduces significantly and the diagnostic resolution even improves with this scheme. A comparison with X-Compact indicates, that simple parity information provides higher diagnostic resolution per response data bit than more complex signatures.**

***Keywords*— Diagnosis, Embedded diagnosis, Multi-site test, Compaction, Design-for-test**

I. Introduction

In multi-site testing, many dies on a load-board or even on a wafer are tested in parallel by the same ATE [1], [2], [3], [4], [5]. All the dies receive identical input by the ATE, but the output side of the die-under-test cannot be handled in the same straightforward way, as the defective dies will respond in many different, unpredictable ways. One solution is feeding all the dies with the correct output by the ATE, equipping them with an on-chip comparator and comparing the expected and computed response on chip (figure 1). In a small on-chip memory the indices of the first n failing vectors or bits are stored and evaluated die by die [1], [6].

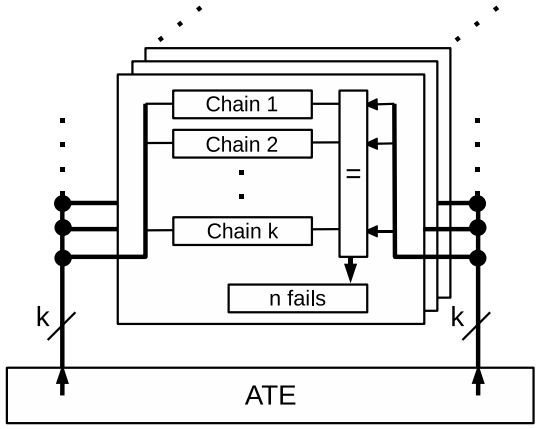

Fig. 1. Principle of multi-site testing.

Throughput requirements and test application time are reduced, if each die is equipped with test data decompression and test response compaction logic (figure 2) [1].

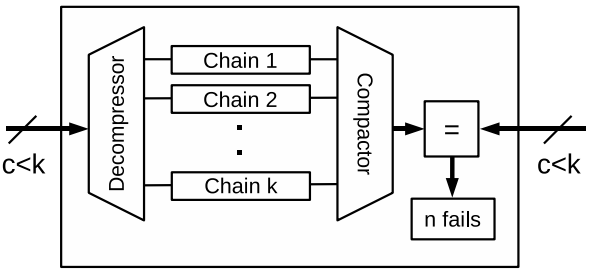

Fig. 2. Test data decompression and response compaction.

While time compactors and convolutional compactors are highly effective in general [7], [8], [9], they are not the optimal choice for implementing a stop-on-nth-fail strategy as the faulty signature is kept over multiple or even all clock cycles, and space compaction techniques are more appropriate [10], [11].

If diagnostic capabilities have to be ensured during BIST, the situation is similar. Here, the correct responses are not provided externally, but must be stored internally in order to implement a stop-on-nth-fail strategy. The complete BIST scheme is shown in figure 3, and again space compaction is the best choice.

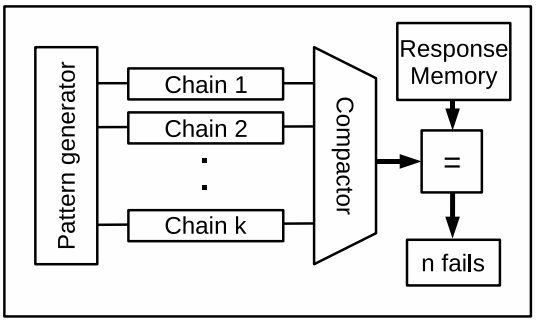

Fig. 3. Built-in self-diagnosis.

The response compaction ratio determines the memory requirements for built-in diagnosis, and the bandwidth for multi-site testing.

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Extreme response compaction is provided by increasing the number of scan chains and hence the test vector length, and by compacting the complete vector into a single parity bit (figure 4).

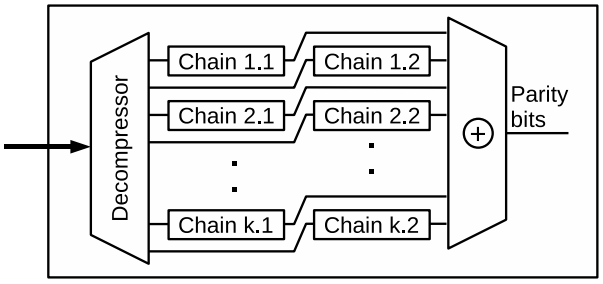

Fig. 4. Extreme response compaction.

The scheme of figure 4 maps a complete vector into a single bit and provides the highest space compaction ratio possible. Experiments in [12] have shown, that this extreme response compaction has only small impact on stuck-at fault coverage and diagnostic resolution for stuck-at faults. However, the goal of a diagnosis algorithm is not just identifying stuck-at faults but to target arbitrary complex defect mechanisms. In addition, embedded and multi-site diagnosis have to be successful by analyzing a rather small number n of failing responses.

Figure 5 shows the extreme compaction scheme applied to multi-site testing and embedded test. Here, merely the expected parity bits are either sent by the ATE or stored on-chip. This significantly reduces the amount of on-chip storage and the ATE bandwidth requirements. The comparator is now a single XOR-gate controlling a memory which records the n first vector indices for which the parity bits mismatch.

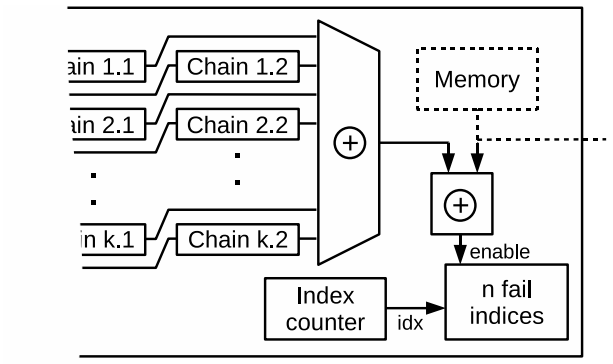

Fig. 5. Target scheme for extreme response compaction.

The goal of this paper is to show, how standard ATPG algorithms have to be adapted for the extreme space compaction scheme, and to present a new pattern analysis algorithm which is able to work just on the parity bits of response vectors and does not target a specific fault model. The outcome of this new technique is beneficial with respect to the uncompacted case under all aspects:

- Shorter test application time due to shorter scan chains.
- Higher defect coverage as more patterns are applied in less time.
- Higher diagnostic resolution since more information is evaluated in less time.
- Need to store a smaller number n of failing responses as longer vectors are compressed into a single bit.

Test data decompression at the input side and unknown values at the outputs are not considered in this paper. Sophisticated techniques for handling the input side of embedded test schemes are published and available on the market. They include continuous reseeding [13], [14], embedded deterministic testing [15], [16], [17], [18]. For masking unknown values prior to parity compaction, several well-known techniques including [19], [20], [21] are applicable here.

The next section deals with adaption of ATPG and diagnosis algorithms to extreme response compaction, section III presents the new fault model independent pattern analysis technique, and section IV reports experimental results with industrial circuits which show that the expectations mentioned above are met indeed.

II. Direct Diagnosis

Three basic approaches can be distinguished for enabling diagnosis with restrictions in bandwidth [22]:

- *Bypassing*: Failing chips are re-tested with disabled response compaction and uncompacted data is transferred to the tester for diagnosis.
- *Indirect diagnosis*: The failing scan cells are calculated out of the compacted data and this reconstructed fail data is used for diagnosis.
- *Direct diagnosis*: Compacted data is diagnosed directly by considering the compaction hardware as part of the design itself.

Bypassing provides full response data but introduces a major test time overhead. It is only suitable during prototyping or precision diagnosis.

Indirect diagnosis requires sufficient information for reconstructing fail data. Many techniques have been proposed which are based on error correcting codes [11], [23], [24], [25], convolutional compactors [7], [26] or special signature registers [8], [9], [27]. To identify a single failing scan cell out of n, at least $\log(n)$ bits must be transferred. Simple parity information is not sufficient. Moreover, reconstructing failure information out of compacted data is error-prone. If the number of failing scan cells exceeds the capabilities of the used code, wrong fail information is reconstructed and diagnosis is mislead.

For extreme space compaction, only the direct diagnosis approach is applicable. Direct diagnosis for extreme compaction is performed by constructing a combinational representation of the circuit under test.

Let k be the number of scan chains, and t the maximum length of a scan chain. All flip-flops which are at the same positions in the scan chains are compressed into a single parity. Hence the combinational representation contains t parity trees each compacting at most k pseudo-primary outputs (figure 6). The

number t now corresponds to the number of parity bits to be evaluated for one test pattern.

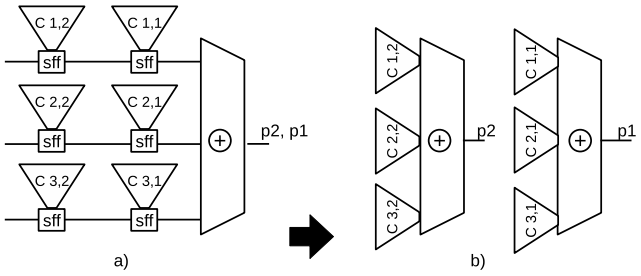

Fig. 6. Combinational representation for extreme response compaction.

The circuit 6b has a higher global reconvergent fan-out in general, a significantly higher fan-in, and is more difficult to test, but the approach rarely introduces new redundancies which would lead to fault masking, and the negative impact can be reduced by an appropriate scan chain organization [28]. However the unusually high fan-in of compactor structures poses a great challenge especially for fault model independent diagnosis approaches. A number of effect-cause [29], [30] approaches rely on cone intersections. The diagnostic resolution of such algorithms decreases and the run times can even double in the presence of a compactor [31]. So far, there is no effect-cause approach available that is fault model independent and specifically designed to handle high-fan-in compactor structures without any degradation in diagnostic resolution.

The combinational representation can be passed to any efficient ATPG-tool, and the test patterns generated this way are input to the pattern analysis algorithm described in the next section.

III. Diagnosis on Parity Information

To analyze extremely compacted response data, we develop a diagnosis algorithm based on the concepts of [32]. The main differences are:

- A per-vector approach is employed instead a per-pattern approach.
- Just the single parity bit is analyzed per vector.
- Analysis has to be completed after observing n erroneous parity bits.

We keep the main benefit of the technique in [32] which is the independence of any fault model assumption by using the *conditional stuck-at line* calculus. A conditional stuck-at line consists of a signal line (the topological part) and an activation condition (the functional part). Figure 7 shows some examples for expressing traditional fault models by using the conditional stuck-at calculus. An arrow represents a conditional stuck-at, its orientation indicates the polarity. Each arrow is annotated with its activation condition. For the crosstalk bridge for instance, the victim line B shows a logic 1 right after a rising transition on aggressor line A.

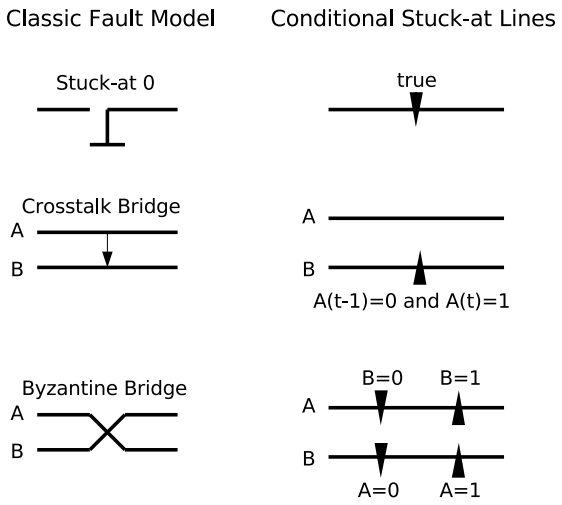

Fig. 7. Examples of conditional stuck-at lines.

The location of the defective region is identified by its conditional stuck-at lines even if the activation condition is unknown. The algorithm described below efficiently generates a ranked list of the most suspect conditional stuck-at lines by successively analyzing the stream of the first $m = n + p$ parity bits (denoted as P_m) of the response with p being the number of passing vectors before the nth failing one. The more response bits are analyzed, the more accurate gets the ranking.

The diagnosis algorithm starts with a fault simulation of all *unconditional* stuck-at lines $f \in F$ in the circuit model. This produces for each stuck-at line f a signature in the form of a m-bit parity bit stream P_m^f. All signatures are compared to the observed parity bits P_m to obtain a ranking of stuck-at lines based on the similarities between their signatures and the observed response. The similarity between a signature P_m^f and the response P_m is expressed by three natural numbers:

- σ_m^f is the number of bit positions faulty both in the response stream P_m as well as in the syndrome P_m^f (predictions).
- ι_m^f is the number of bit positions correct in P_m but faulty in P_m^f (mispredictions).
- τ_m^f is the number of bit positions faulty in P_m but correct in P_m^f (nonpredictions).

If the real culprit behaves like an unconditional stuck-at fault f, we get $\iota_m^f = \tau_m^f = 0$ and σ_m^f will be maximum. If the fault in the DUD is not always active due to indeterministic behavior or some unknown activation mechanism it can be described with a *conditional* stuck-at fault f'. Even in this case, f predicts all failing responses and σ_m^f is still maximum with respect to all other faults $g \in F$. Consequently, a location with more predictions gets ranked higher:

$$\sigma_m^a > \sigma_m^b \Rightarrow \mathit{rank}(a) > \mathit{rank}(b).$$

For a conditional fault, the value ι_m^f (the number of mispredictions) will not be zero any more and is used in addition for ranking fault candidates. The lower ι_m^f, the higher is the frequency of the activation condition and the more likely the

particular conditional stuck-at line. Therefore, evidences with identical σ_m^f are ordered by increasing ι_m^f:

$$\iota_m^a < \iota_m^b \Rightarrow \mathit{rank}(a) > \mathit{rank}(b).$$

The main benefit of this processing with respect to the SLAT [33] and other algorithms is in the fact that not only failing but also all passing vectors are evaluated until the nth failing parity bit is obtained.

Extreme space compaction has no impact on the effect-cause approach described above. It is based only on fault simulation, summation and sorting. As for fault simulation, standard acceleration techniques from cause-effect approaches like fault dictionaries can also be used here to cache the (compacted) syndromes of conditional stuck-at lines. The approach is therefore perfectly suitable for high-volume applications.

Each defect corresponds to a set of identifying evidences pointing out its victim signal lines. We count a diagnosis of a defect as success, if and only if the top-ranked evidence corresponds to the defect and no non-identifying evidence has the same confidence. If the resulting candidate ranking is not perfect in this sense, we consider the diagnosis a fail. This rigid definition of diagnostic success is suitable for benchmarking the algorithm because the resulting figures form a lower bound to the success rates expected in different applications. Depending on the diagnosis environment, additional candidates from top of the ranking can be considered. This consideration may only improve the success rates.

IV. Experimental Results

We performed a series of experiments to analyze the impact of extreme space compaction on industrial designs and to validate the performance of the diagnosis algorithm presented above.

The industrial designs were provided by NXP, and table I shows their characteristics. The design name in the first column corresponds to the number of logic gates. The next columns show the number of scan elements (*sff*), the number of scan chains (k) and the length of the longest scan chain (t).

ATPG was performed on these original designs without any compaction by using a commercial tool. The number of test patterns and the corresponding stuck-at fault coverage are reported in columns p and fc. The test time is determined by the number of shifting cycles necessary to apply the test set. The number of shifting cycles equals the number of test patterns p multiplied by the length of the longest scan chain t, reported in column $p \cdot t$.

In each shifting cycle, k response bits are observed at the output of the scan chains. Therefore, column $p \cdot t \cdot k$ gives the number of response bits. For example over 7 million shift cycles are necessary for the p295k and the amount of response data rises up to 124 Mbit for the p418k.

Two series of experiments were conducted. First, we report the reduction of response data, gain in test time and improved diagnostic success obtained by extreme response compaction.

design	*sff*	k	t	p	$p \cdot t$	$p \cdot t \cdot k$	fc
p100k	5829	18	792	2053	1625976	29267568	99.51
p141k	10502	24	486	1643	798498	19163952	98.88
p239k	18495	40	541	1080	584280	23371200	98.78
p259k	18495	40	541	1228	664348	26573920	99.08
p267k	16621	45	494	1122	554268	24942060	99.60
p269k	16621	45	494	1115	550810	24786450	99.60
p279k	17827	55	416	1305	542880	29858400	97.90
p286k	17827	55	416	2133	887328	48803040	98.41
p295k	18521	11	1852	3868	7163536	78798896	99.16
p330k	17468	64	317	5332	1690244	108175616	98.96
p378k	17420	325	64	82	5248	1705600	100.00
p388k	24065	50	546	982	536172	26808600	99.47
p418k	29809	64	831	2350	1952850	124982400	98.36
p469k	403	1	706	320	225920	225920	98.81
p483k	32610	71	900	487	438300	31119300	98.84

TABLE I
Circuit characteristics and fault coverage obtained by a commercial tool

Then, we investigate the relationship between diagnostic success and response data volume for both X-Compact [11] and extreme space compaction.

The original scan chains have been split into multiple shorter chains in order to reach a ratio of approximately $k \sim 5t$. This wide scan chain organization with rather short chains will reduce test time significantly. The first columns of table II show the number of scan chains k and maximum scan chain length t of the new configurations. Now, parity trees were attached to the designs and the same ATPG run was performed on the corresponding combinational representations.

The commercial ATPG was not able to compact the test sets as much as with the original designs. So the number of test patterns (column p) is higher in almost every case. However, as the scan chain lengths are much shorter now, the number of shifting cycles *decreases* and an average test time improvement of 4.2X is obtained (see column Δt). The test time did not improve for p378k, because the original scan chain configuration of this design already satisfies $k \sim 5t$ and no splitting was performed.

In each shifting cycle, only one response bit has to be observed at the output, hence the number of response bits equals the number of shifting cycles (column $p \cdot t \cdot 1$) and the response data volume is reduced by several orders of magnitude (column Δr). As expected, the fault masking introduced by the compactor is negligible. Column Δfc shows a slight reduction in stuck-at fault coverage for some circuits, which is mainly attributed to a larger number of faults aborted by the ATPG. and fault coverage may even increase due to the higher pattern count. The average values reported at the end of each table are weighted averages where each number is weighted with the relative size of the corresponding circuit in gates.

The diagnosis algorithm presented above works independently of a fault model, however, its performance can be validated by complex fault assumptions.

For each of the designs, we diagnosed a randomly selected sample of 4000 faults. Each sample consists of 1000 stuck-at faults, 1000 crosstalk faults, 1000 delay faults and 1000 single-victim wired-and bridges. As the ATPG only targeted stuck-at

design	k	t	p	$p \cdot t \cdot 1$	Δt	Δr	Δfc
p100k	270	53	2203	116759	13.9X	250X	0.01
p141k	264	45	3059	137655	5.8X	139X	0.01
p239k	360	61	3494	213134	2.7X	109X	0.00
p259k	360	61	4259	259799	2.6X	102X	0.00
p267k	360	62	5363	332506	1.7X	75X	0.04
p269k	360	62	5348	331576	1.7X	74X	0.04
p279k	385	60	5960	357600	1.5X	83X	0.00
p286k	385	60	7006	420360	2.1X	116X	0.00
p295k	329	62	6942	430404	16.6X	183X	0.00
p330k	320	64	9105	582720	2.9X	185X	0.03
p378k	325	64	176	11264	0.5X	151X	0.01
p388k	400	69	4237	292353	1.8X	91X	0.00
p418k	576	93	7991	743163	2.6X	168X	0.01
p469k	60	12	316	3792	59.6X	59X	0.01
p483k	568	113	3425	387025	1.1X	80X	0.02
avg.					4.2X	121X	0.01

TABLE II

REDUCTION OF TEST TIME AND RESPONSE DATA VOLUME WITH EXTREME COMPACTION

	stuck-at faults		non-target faults	
design	orig.	parity	orig.	parity
p100k	84.0%	84.2% +0.2	81.4%	81.2% –0.2
p141k	88.1%	88.6% +0.5	83.7%	83.5% –0.1
p239k	85.9%	85.9% +0.0	86.3%	87.5% +1.2
p259k	87.3%	87.8% +0.4	86.7%	88.7% +2.0
p267k	86.5%	88.4% +1.9	79.9%	86.2% +6.3
p269k	86.5%	87.0% +0.5	82.8%	85.3% +2.6
p279k	84.7%	87.6% +2.9	77.8%	81.0% +3.3
p286k	83.8%	85.7% +1.9	76.0%	79.3% +3.3
p295k	79.7%	80.4% +0.7	72.1%	71.5% –0.6
p330k	79.9%	81.0% +1.1	82.4%	84.4% +2.0
p378k	81.3%	81.6% +0.3	72.9%	76.2% +3.3
p388k	88.3%	88.9% +0.6	85.9%	89.0% +3.1
p418k	87.3%	87.8% +0.5	82.2%	84.2% +2.1
p469k	51.5%	51.8% +0.3	54.0%	52.7% –1.3
p483k	86.2%	86.2% +0.0	83.5%	87.7% +4.2
avg.	84.5%	85.3% +0.8	80.6%	83.2% +2.5

TABLE III

IMPROVEMENTS IN DIAGNOSTIC SUCCESS BY ANALYZING ONLY THE PARITY BITS

faults, we'll refer to the other faults as *non-target faults*.

Table III compares the diagnostic success rates on the full uncompacted response with the diagnosis on the complete parity bit stream ($m = p \cdot t$). The last row shows the averages weighted by the design sizes. We observe an improvement in diagnostic success even with only 1/100th of the response data available. This shows, that the analysis of a single parity bit provides the same diagnostic resolution as 100+ uncompacted response bits. For non-target faults, the diagnostic resolution improves even further because the larger test set has higher defect coverage.

In the second series of experiments, we aim to compare the storage and bandwidth requirements of X-Compact and parity compaction. The X-Compactor can be parametrized by the number u of tolerated unknowns in a vector. As a parity tree does not tolerate any unknowns, we set $u = 0$ for a fair comparison. The resulting compactor guarantees error detection, if a vector contains one, two or any odd number of fails. In addition, if only one or two failing bits are present, these bits can be located by the signature. For vector length between 257 and 512, the X-Compact signature is 10 bits long. For embedded diagnosis, the signatures must be stored in an on-chip response ROM, and for multi-site testing, the signatures must be provided by the tester just-in-time. The response memory per shifting cycle is reduced by a factor of 10X by using parity compaction with a single bit. For multi-site testing, the bandwidth needed for providing the correct signatures is reduced by a factor of 10X, too. While in multi-site testing the first n failing vector indices for extreme response compaction and the first n failing vector indices + 10 bits per vector for the signature have to be stored, embedded diagnosis requires storing the parity bits of all the vectors or all the 10 bit signatures.

As a single X-Compact signature provides more diagnostic information than a parity bit, fewer X-Compact signatures may be needed to reach a certain diagnostic success.

To compare the fails storage requirements we use the straight forward encoding. For each fail, a 20 bit vector index and the signature is stored. In the case of X-Compact, 30 bits are needed to store a fail, and for parity compaction, only the 20 bit vector index is needed. We replaced the parity trees with X-Compact structures and performed diagnosis on its codewords. In addition, we recorded the amount of fail data analyzed during diagnosis to obtain the expected success rates with given fails memory size.

Figure 8 show the average diagnostic success on the complete fault samples to be expected with a given amount of fail data.

With limited amount of fails memory the success rate of extreme response compaction is significantly higher than the one obtained by X-Compact. So storing just the indices of failing vectors is more efficient than spending additional memory for X-Compact signatures. The two markings in figure 8 denote the break-even points where the diagnostic success with compaction reaches the diagnostic success on the full, uncompacted response data of the original designs. For extreme compaction $n = 165$ failing vector indices need to be stored which requires 3300 bits of memory. At these break-even points the fails memory for parity compaction is still smaller than for X-Compact. If we assume unlimited on chip resources, the diagnostic success rate is higher with X-Compact as expected.

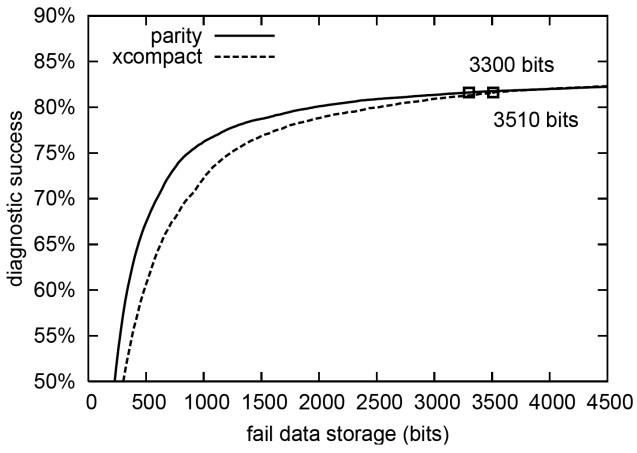

Fig. 8. Diagnostic success with limited amount of fail data

V. Conclusions

Extreme space compaction is obtained by increasing the number of scan chains and compressing them into a single parity bit. This compaction scheme is especially suited for BIST and multi-site testing. A direct diagnosis approach has been presented, that is suited for extreme compaction. The experimental results on industrial designs have shown, that test time and response data volume reduces significantly and the diagnostic resolution even improves with this scheme. In comparison to X-Compact, the response data is reduced by a factor of 10X and less fails data storage is needed to retain diagnostic resolution.

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