Structural-Based Power-Aware Assignment of Don't Cares for Peak Power Reduction during Scan Testing

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***Abstract*—Scan architectures, though widely used in modern designs for testing purpose, are expensive in power consumption. In this paper, we first discuss the issues of excessive peak power consumption during scan testing. We next show that taking care of high current levels during the test cycle (i.e. between launch and capture) is highly relevant so as to avoid noise phenomena such as IR-drop or Ground Bounce. Then, we propose a solution based on power-aware assignment of don't care bits in deterministic test patterns that considers structural information of the circuit under test. Experiments have been performed on ISCAS'89 and ITC'99 benchmark circuits with the proposed structural-based power-aware X-filling technique. These results show that the proposed technique provides the best tradeoff between peak power reduction and increase of test sequence length.**

I. INTRODUCTION

While many techniques have evolved to address power minimization during the functional mode of operation, it is now mandatory to manage power during test mode. Circuit activity is substantially higher during test than during functional mode, and the resulting excessive power consumption can cause structural damage or severe decrease in reliability of the circuit under test [1, 2, 3, 4]. In the context of scan testing, the problem of excessive power during test is much more severe as the application of each test pattern requires a large number of shift operations that contributes to unnecessarily increasing the switching activity [2].

Power consumption must be analyzed from two different perspectives. Average power consumption is, as the name implies, the average power utilized over a long period of operation or a large number of clock cycles. Instantaneous power is the amount of power required during a small instant of time such as the portion of a clock cycle immediately following the system clock rising or falling edge. The peak power is the maximum value of the instantaneous power.

Average power consumption during scan testing can be controlled by reducing the scan clock frequency – a well known solution used in industry. In contrast, peak power consumption during scan testing is independent of the clock frequency and hence is much more difficult to control. As reported in recent industrial experiences [3], scan patterns in some designs may consume much more peak power over the normal mode and may result in failures during manufacturing test. Combined with high speed, excessive peak power during test also causes high rates of current (di/dt) in the power and ground rails and hence leads to excessive power and ground noise (V_{DD} or Ground bounce). This may erroneously change the logic state of some circuit nodes or flip-flops and cause some good dies to fail the test, thus leading to unnecessary loss of yield. Similarly, IR-drop and crosstalk effects are phenomena that may show up an error in test mode but not in functional mode. With high peak current demands during test, the voltages at some gates in the circuit are reduced. This causes these gates to exhibit higher delays, possibly leading to test fails and yield loss [5].

The problem of excessive peak power during scan testing can be divided in two sub-problems: excessive peak power during load/unload cycles and excessive peak power during the test cycle, denoted as TC and defined as the clock cycle between launch and capture.

Several techniques have been proposed for reducing test power dissipation during load/unload cycles [6]. Most of them are initially targeted for reducing average power but they usually can reduce peak power as well. The low power scan architectures proposed in [7, 8] reduce the clock rate on the scan cells during shift operations thus reducing the power consumption without increasing the test time. The technique presented in [9] consists in splitting the scan chain into a given number of length-balanced segments and in enabling only one scan segment during each clock cycle of the scan process. The solutions proposed in [10, 11] consist in assigning don't care bits of the deterministic test cubes used during test in such a way that it can reduce the peak power.

Compared to load/unload cycles, peak power reduction during TC is a less researched yet more challenging area. In this case, the problem is that TC is generally operated at-speed for high defect detection while load/unload cycles are

generally operated at a lower speed for power consumption reason. Therefore, a high peak power during TC may lead to a situation where gates in the circuit exhibit higher delays [5], so that erroneous data may be captured in the scan chain at the end of TC. A possible solution to reduce peak power during TC is to use scan cell reordering [12, 13]. The main drawback of this technique is that power-driven chaining of scan cells cannot guarantee short scan connections and prevent congestion problems during scan routing. Another solution proposed in [14] is based on appropriately filling Xs of deterministic test cubes with values that can ensure low switching activity during TC. However, this technique is only applicable to specific and non classical clock schemes such as the launch-off-capture clock scheme used to target delay faults during scan.

In this paper, we propose solutions based on power-aware assignment of don't care bits in deterministic patterns that can efficiently reduce peak power during TC. From a set of deterministic test cubes, the proposed solution fills Xs with specific values (0, 1 or MT-filling) that minimizes the occurrence of transitions and hence the peak power during TC. Compared to other solutions, such X-filling technique has the advantage to be applicable after the end of the design process and thus do not require any modification of the circuit and hence any area overhead. Despite its effectiveness in reducing peak power during TC, this "classical" solution has the disadvantage of providing results that may vary according to the structure of the circuit under test. To overcome this problem, we propose a novel X-filling technique that consists in assigning Xs by considering structural information of the circuit under test. This technique, called Structural-Based power-aware X-filling (SB-filling), consists in assigning Xs with values that guarantee the stability of the output of the first level of gates connected to the scan chain. As it will be shown in the last section of the paper, the SB-filling technique provides the best tradeoff between peak power reduction and increase of test length.

The remainder of the paper is organized as follows. In the next section, we analyze peak power during the test cycles of scan testing and we highlight the importance of reducing this component of the power. In Section 3, we present the peak power reduction achieved with the classical X-filling technique. Section 4 presents the new SB-filling technique. In addition to results obtained with the proposed technique on peak power reduction during TC, Section 5 presents results on peak power reduction during load/unload cycles. Section 6 concludes this paper.

II. PEAK POWER DURING SCAN

During conventional scan testing, each test vector is first scanned into the scan chain(s). After a number of load clock cycles, a last shift in the scan chain launches the test vector. The scan enable (SE) signal is disabled, thus allowing the test response to be captured/latched in the scan chain(s) at the next clock pulse (see Figure 1). After that, SE is switched on, and the test response is scanned out as the next test vector is scanned in.

There can be a peak power violation (peak power exceeding a specified limit) during either the load/unload cycles or during TC. In both cases, a peak power violation can occur because the number of flip-flops that change value in each clock cycle can be really higher than that during functional operation. In [4], it is reported that only 10-20 % of the flip-flops in an ASIC change value during one clock cycle in functional mode, while 35-40 % of these flip-flops switch during scan testing.

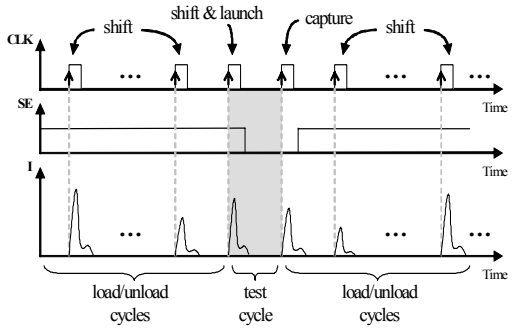

Figure 1. Scan testing and current waveform

In order to analyze when peak power violation can occur during scan testing, we conducted a set of experiments on benchmark circuits. Considering a single scan chain composed of *n* scan cells and a deterministic test sequence for each design, we measured the current consumed by the combinational logic during each clock cycle of the scan process. We pointed out the maximum value of current during the *n* load/unload cycles of the scan process and during TC (which last during a single clock cycle). Note that current during TC is due to transitions generated in the circuit by the launch of the deterministic test vector (see Figure 1).

Identification of peak power violation cannot be done without direct comparison with current (or power) measurements made during functional mode. However, this would require knowledge of functional data for each benchmark circuit. As these data are not available, the highest values of current we pointed out are not necessarily peak power (current) violations. They are simply power (current) values that can lead to peak power (current) violation during scan testing. Reports made from industrial experiences have shown that such violations can really occur during manufacturing scan testing [3, 4].

The benchmarking process was performed on circuits of the ISCAS'89 and ITC'99 benchmark suites. We report in Table 1 the main features of these circuits. For each experimented circuit, we give the number of scan cells, the number of gates, the number of deterministic test patterns and the associated fault coverage (FC). All experiments are based on deterministic testing from an ATPG tool "TetraMAX™" of Synopsys [15]. The missing faults in the FC column are redundant or aborted faults. Primary inputs

and primary outputs were not included in the scan chain, but were assumed to be held constant during scan-in and scan-out operations. Random initial logic values were assumed for the scan flip-flops.

TABLE 1 FEATURES OF EXPERIMENTED CIRCUITS

Circuit	# scan cells	# gates	# patterns	FC (%)
b10	17	155	44	100
b11s	31	437	62	100
b12	121	904	94	100
b13s	53	266	30	100
b14s	245	4444	419	99.52
b17s	1415	22645	752	98.99
s1196	18	529	137	100
s5378	179	2779	151	100
s9234	228	5597	161	99.76
s13207	669	7951	255	99.99
s38417	1636	22179	145	100

Results concerning peak power consumption are given in Table 2. We have reported the peak power (expressed in milliWatts) consumed during the load/unload cycles (second column), and that consumed during TC (third column). These values represent the maximum over the entire test sequence. Power consumption in each circuit was estimated by using PowerMill® of Synopsys [16], assuming a power supply voltage of 2.5 Volts and technology parameters extracted from a 0.25µm digital CMOS standard cell library.

TABLE 2 PEAK POWER DURING SCAN TESTING

Circuit	Peak power consumption (mW)	
	load/unload cycles	test cycle (TC)
b10	27.88	23.71
b11s	50.42	41.27
b12	113.84	101.46
b13s	61.09	52.92
b14s	395.55	319.83
b17s	1038.35	1118.68
s1196	66.89	10.03
s5378	197.76	179.66
s9234	359.68	339.88
s13207	499.68	483.30
s38417	1121.80	1074.33

These results show that peak power consumption is always higher during the load/unload cycles than during TC. This result was quite predictable as the number of clock cycles during the load/unload phase is much more than one. More importantly, these results show that even if peak power is higher during the load/unload cycles, peak power during TC is in the same order of magnitude. This may lead to problematic noise phenomena during TC. Let us consider again the IR-drop phenomenon. It is due to a high peak current demand that reduces the voltages at some gates in the CUT and hence causes these gates to exhibit higher delays. The gate delays do not affect the load/unload process as no value has to be captured/stored during this phase. Conversely, the gate delays can really affect TC because the values of output nodes in the combinational logic have to be captured in the scan flip-flops. As this operation is generally performed at-speed, this phenomenon is therefore likely to occur during this phase and negatively impact test results and thus yield. We can therefore conclude that taking care of peak power during TC and trying to minimize the switching density of the circuit during this phase are really relevant and require new development of dedicated techniques.

III. CLASSICAL RANDOM X-FILLING HEURISTICS

In conventional ATPG, don't care bits (Xs) are filled in randomly, and then the resulting fully specified pattern is simulated to confirm detection of all targeted faults and to measure the amount of "fortuitous detection" – faults which were not explicitly targeted during pattern generation but were detected anyway. It is interesting to note that the fraction of don't care bits in a given pattern is nearly always a very large fraction of the total available bits [17, 18]. This observation remains true despite the application of state-of-the-art dynamic and static test pattern compaction techniques. The significant fraction of don't care bits presents an opportunity that can be exploited for power minimization during scan testing. In addition, this solution avoids congestion problems inherent to scan chain modification techniques and allows at-speed testing.

In order to reduce peak power during TC, the idea in this work is to use a test generation process during which non-random filling is used to assign values to don't care bits (Xs) of each test pattern of the deterministic test sequence. First, the Xs are assigned with the help of the following classical non-random filling heuristics:

- *Adjacent filling* also called *MT-filling* (Minimum Transition filling): all don't care bits in a pattern are set to the value of the last encountered care bit.
- *0-filling*: all don't care bits in a pattern are set to '0'.
- *1-filling*: all don't care bits in a pattern are set to '1'.

For example, consider the single test pattern 0XXX1XX0XX0XX. If we apply each of the three non-random filling heuristics, the resulting patterns will be:

- 0000111000000 with MT-filling.
- 0000100000000 with 0-filling,
- 0111111011011 with 1-filling,

These classical non-random filling heuristics (among few others) have been evaluated in [5] to measure the reduction in average power consumption during scan shifting (load/unload cycles). Results reported in [5] indicate that the MT-filling technique does an excellent job in lowering overall switching activity while still maintaining a reasonable increase in patterns count. From our side, we have evaluated these heuristics to measure the reduction in peak power consumption during TC with respect to a random filling of don't care bits.

Results of the experiments performed on ISCAS'89 and ITC'99 benchmark circuits are reported in Table 3. For each circuit, we report the reduction achieved by each classical X-filling heuristic compared to the standard random-filling. The values in bold correspond to the best results. Complete results on benchmark circuits have shown that peak power reduction of up to 89% can be achieved with the MT-filling technique.

TABLE 3 PEAK POWER REDUCTION DURING TC

Circuits	MT-Filling	0-Filling	1-Filling
b10	**40.4**	7.3	23.4
b11s	**20.6**	19.2	7.6
b12	67.5	**68.2**	57.8
b13s	**60.0**	43.9	49.7
b14s	26.3	**30.7**	-10.7
b17s	**80.1**	77.7	75.7
s1196	**79.3**	58.2	66.1
s5378	**74.2**	67.5	70.7
s9234	**66.5**	44.6	41.6
s13207	**89.5**	84.4	87.9
s38417	71.8	82.5	**84.1**

These results show the efficiency of the experimented heuristics in terms of peak power reduction during TC. Most of the time, the MT-filling heuristic performs better than the others as it ensures less activity in the scan chain. But this is not always true as the structural properties of a given circuit may sometimes favor one heuristic rather than another. For example, circuit b14s has more than 500 AND/NAND gates connected to the flip-flops, while it has only 47 OR/NOR gates. In these conditions, it was highly predictable that the 0-filling heuristic performs better for this circuit. This is confirmed by the results in Table 3 where the 0-filling induces a 30.7% reduction instead of a 10.7% increase for the 1-filling. This observation is used to propose a more efficient X-filling heuristic considering structural information of the circuit under test.

IV. STRUCTURAL-BASED POWER-AWARE X-FILLING

In the previous section, we have shown that a power-aware assignment of don't care bits in a deterministic test sequence is a promising solution to reduce peak power during TC. However, the performance of the classical X-filling heuristics is dependent on the circuit structure, *i.e.* the type of gates driven by the flip-flops. Therefore, the Structural-Based power-aware X-filling (SB-filling) technique presented in this section consists in assigning Xs according to such type of structural information. Compared to the previous X-filling heuristics that minimize the number of transition in the scan chain, the SB-filling technique reduce the number of transition in the CUT by keeping stable the outputs of gates directly connected to the scan flip-flops.

Depending on the type of gates directly connected to the scan flip-flops, the Xs will be filled so as to block possible transitions in the combinational part of the circuit. Let us consider the circuit presented in Figure 2. In this example, gate G1 has its two inputs directly fed by the scan chain while gate G2 has only one input connected to a flip-flop.

In order to ensure the stability (no transition) of gate G1, we have to satisfy the following equation:

$$\overline{Y_i}\cdot\overline{Y_{i+1}} + \overline{Z_i}\cdot\overline{Z_{i+1}} + \overline{Y_i}\cdot\overline{Z_{i+1}} + \overline{Z_i}\cdot\overline{Y_{i+1}} + Y_i\cdot Y_{i+1}\cdot Z_i\cdot Z_{i+1} = 1 \quad (1)$$

Each term of Eq. 1 corresponds to a succession of values at the inputs of the gate that guarantee its output's stability. The two first terms $\overline{Y_i}\cdot\overline{Y_{i+1}}$ and $\overline{Z_i}\cdot\overline{Z_{i+1}}$ correspond to a succession of two '0s' on the same input. The two following ones ($\overline{Y_i}\cdot\overline{Z_{i+1}}$ and $\overline{Z_i}\cdot\overline{Y_{i+1}}$) can also ensure the stability at the gate's output but may induce a glitch on the output. The presence of a glitch depends on the propagation delay from the output of the flip-flops to the input of the gate. As flip-flops connected to gates are normally close in the layout, the delay of both paths has a high probability to be balanced. Moreover, if the glitch appears, its energy will not be large enough to be propagated deeply in the circuit. Finally, the last term $Y_i\cdot Y_{i+1}\cdot Z_i\cdot Z_{i+1}$ means that all the inputs stay at '1' in order to obtain a stable '1' at the gate's output.

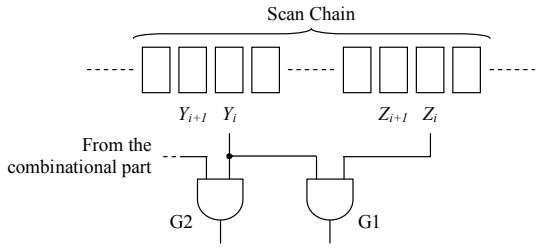

Figure 2. Example of gates connected to a scan chain

In order to deal with this satisfiability (SAT) based problem, Eq. 1 is rewritten as a product of sums. Each term is called a "clause" and has to be satisfied in order to guarantee the stability of the gate's output. Eq.1 becomes:

$$\left(\overline{Y_i} + \overline{Z_i} + Y_{i+1}\right)\cdot\left(\overline{Y_i} + \overline{Z_i} + Z_{i+1}\right)\cdot \left(\overline{Y_{i+1}} + \overline{Z_{i+1}} + Y_i\right)\cdot\left(\overline{Y_{i+1}} + \overline{Z_{i+1}} + Z_i\right) = 1 \quad (2)$$

Now, if the gate is driven by only one scan flip-flop (gate G2 in Figure 1) and the others inputs come from the combinational part, the equation that has to be satisfied is the following:

$$\overline{Y_i}\cdot\overline{Y_{i+1}} = 1 \quad (3)$$

which indicates that a succession of two '0s' guarantees the stability at the gate's output.

For a complete analysis, we have to compute such equations for all gates directly driven by scan flip-flops and

for all test vectors in the test sequence. If the gate is an inverter, we consider the gate connected to the output of the inverter as directly connected to the scan flip-flop with an inverted input. Table 4 gives the satisfiability equations for classical 2-input gates. Similar equations can be easily obtained for gates with three or more inputs. Note that XOR or NXOR gates directly connected to the scan chain can be transformed in primitive gates.

The SB-filling technique starts from this set of equations. The problem we have to solve is similar to a SAT problem. A straightforward approach should consist in using a SAT solver to verify if all the clauses can be satisfied simultaneously. But considering the negligible probability of such a case, we rather propose a solution that guarantees the stability at the output of a maximum number of gates. As the resolution of such a problem is NP-complete, we use the greedy algorithm presented in Figure 3.

```
Find the gates connected to the scan chain;
Compute the equation for each gate;
Run a deterministic generation with non-random fill;
For each pattern of test sequence {
    Update the equations with the specified bits;
    For each 'X' bit {
        Assign a '0' to the 'X' {
            Compute the number of equations satisfied (n0);
            Compute the remaining number of equations (p0);
            Compute the remaining total number of clauses (nc0);
        }
        Assign a '1' to the 'X' {
            Compute (n1), (p1) and (nc1);
        }
        if (n0 > n1)        Replace 'X' with a '0';
        else if (n1 > n0)   Replace 'X' with a '1';
        else if (p0 > p1)   Replace 'X' with a '0';
        else if (p1 > p0)   Replace 'X' with a '1';
        else if (nc0 > nc1) Replace 'X' with a '1';
        else if (nc1 > nc0) Replace 'X' with a '0';
        else                Replace 'X' with the adjacent
                            filling technique;
        Update the equations;
    }
}
Run a fault simulation to remove the unnecessary patterns;
Run the peak power evaluation during TC;
```

Figure 3. Greedy algorithm

From the set of equations computed for each gate directly connected to the scan chain, the internal loop of the algorithm is executed for each pattern of the test sequence. We first use the specified bits of the pattern in order to update the equations of each gate. Then, we start from the first X of the pattern. The X is first set to '0' and next to '1'. We compute the number of equations satisfied (n), the remaining number of equations that have to be satisfied (p) and finally the remaining total number of clauses in all the equations (nc). From these three values, the assignment of Xs is chosen according to the following rules applied successively:

- Maximize the number of satisfied equations.
- Maximize the remaining number of equations.
- Minimize the remaining total number of clauses.
- Finally, if no solution is found, the X is set with the MT-filling heuristic

Then the equations are updated with the selected value and the following X is considered. When all the Xs of the test sequence are assigned to a specific value, the resulting test sequence is simulated in order to remove possible unnecessary patterns. This sequence is used to evaluate the peak power reduction during TC compared to a deterministic test sequence generated with random-filling. Note that these X-filling techniques can be implemented in an ATPG tool.

TABLE 5 PEAK POWER REDUCTION WITH SB-FILLING

Circuit	SB-Filling	MT-Filling	0-Filling	1-Filling
b10	39.4	**40.4**	7.3	23.4
b11s	**20.9**	20.6	19.2	7.6
b12	**70.1**	67.5	68.2	57.8
b13s	53.3	**60.0**	43.9	49.7
b14s	27.2	26.3	**30.7**	-10.7
b17s	78.9	**80.1**	77.7	75.7
s1196	66.3	**79.3**	58.2	66.1
s5378	**74.2**	**74.2**	67.5	70.7
s9234	43.8	**66.5**	44.6	41.6
s13207	85.3	**89.5**	84.4	87.9
s38417	52.5	71.8	82.5	**84.1**
Av.	52.4	**55.9**	50.2	44.5
St. dev.	**21.4**	24.8	25.6	32.6
TL inc.	**4.4 %**	4.6 %	15.9 %	16.1 %

As for the classical X-filling heuristics, the experiments were performed on ISCAS'89 and ITC'99 benchmark circuits. Results are shown in Table 5 where, for each circuit, we report the peak power during TC and the reduction obtained with the SB-filling heuristic. The three last columns of Table 5 remind the reductions achieved with the classical

TABLE 4 SATISFIABILITY EQUATIONS THAT GUARANTEE THE OUTPUT STABILITY FOR AND, NAND, OR AND NOR GATES

Gate type	Connection	Satisfiability equations that guarantee output stability
AND NAND	with two inputs directly connected to the scan chain	$\left(\overline{Y_i} + \overline{Z_i} + Y_{i+1}\right) \cdot \left(\overline{Y_i} + \overline{Z_i} + Z_{i+1}\right) \cdot \left(\overline{Y_{i+1}} + \overline{Z_{i+1}} + Y_i\right) \cdot \left(\overline{Y_{i+1}} + \overline{Z_{i+1}} + Z_i\right) = 1$
	with only one input directly connected to the scan chain	$\overline{Y_i} \cdot \overline{Y_{i+1}} = 1$
OR NOR	with two inputs directly connected to the scan chain	$\left(Y_i + Z_i + \overline{Y_{i+1}}\right) \cdot \left(Y_i + Z_i + \overline{Z_{i+1}}\right) \cdot \left(Y_{i+1} + Z_{i+1} + \overline{Y_i}\right) \cdot \left(Y_{i+1} + Z_{i+1} + \overline{Z_i}\right) = 1$
	with only one input directly connected to the scan chain	$Y_i \cdot Y_{i+1} = 1$

X-filling heuristics. The three rows report the average reduction, the standard deviations and the increase of test length respectively. Note that, the computation time of the SB-Filling technique is about few seconds for small circuit and less than 2 minutes for the biggest circuits.

From these results two conclusions can be drawn. First, the SB-Filling heuristic achieved a 52.4% reduction in average compared to the maximum of 55.9% reduction achieved with MT-filling. Although SB-filling is not the mean best solution, i) it provides for each circuit a reduction close or equal to the best one and ii) the obtained results exhibit the lowest standard deviation (St. dev.). In other words, SB-filling guarantees that each circuit has good peak power reduction whereas the reductions achieved by the classical X-filling heuristics are more variable. Moreover, the SB-filling heuristic is the least expensive in terms of test time as it involves the minimum increase of test length compared to a deterministic test sequence with random-filling (see line TL inc. in Table 5).

V. PEAK POWER REDUCTION DURING LOAD/UNLOAD

As previously mentioned, an excessive peak power during TC may induce delays in the combinational part. The data that have to be captured at the end of TC may hence be corrupted in presence of a high peak power. Then, the X-filling solutions presented earlier can be used to solve this problem. In addition, an advantageous side-effect of the X-filling heuristics is that they reduce peak power during load/unload cycles as well (Table 6). For ISCAS'89 and ITC'99 benchmarks circuits SB-filling achieves the best peak power reduction during load/unload cycles.

TABLE 6 PEAK POWER REDUCTION DURING LOAD/UNLOAD

Circuit	SB-Filling	MT-Filling	0-Filling	1-Filling
b10	17.73	**20.75**	11.33	12.39
b11s	18.78	10.87	**19.13**	2.46
b12	**58.68**	58.43	57.17	51.05
b13s	**45.73**	39.72	42.79	32.56
b14s	37.24	19.53	**42.44**	6.31
s1196	6.66	7.84	9.35	**11.09**
s5378	52.66	52.58	45.04	**57.24**
s9234	31.97	**34.06**	31.33	30.51
Average	**31.8**	28.4	30.7	23.5

Consequently, SB-filling is the solution that provides the best tradeoff between peak power reduction (the lowest standard deviation of peak power reduction during TC and the maximum peak power reduction during load/unload) and the increase of test length. In addition, this technique does not require any modification of the basic design of the circuit and no additional DfT features are required to implement this solution. Finally, at-speed testing is possible so that the defect coverage of the initial test sequence can be maintained.

VI. CONCLUSION

In this paper, we have shown that excessive peak power consumption during all test cycles of scan testing has to be controlled to avoid noise phenomena such as IR-drop or ground bounce. Without caution, these phenomena may lead to yield loss during manufacturing test as test cycles are generally operated at-speed. Our main goal in this paper was to minimize the peak power consumption during these test cycles.

The reduction of peak power during TC can be addressed from different perspectives. In this paper, we have proposed a structural-based power-aware X-filling technique to assign don't care bits of deterministic test patterns. Compared to classical X-filling heuristics, the SB-filling solution is the most attractive as it leads to the best tradeoff between peak power reduction and increase of test length. In addition, no modification of the basic design of the circuit and no additional DfT features are required.

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