

# A Modified Clock Scheme for a Low Power BIST Test Pattern Generator

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**Abstract:** *In this paper, we present a new low power BIST test pattern generator that provides test vectors which can reduce the switching activity during test operation. The proposed low power/energy BIST technique is based on a modified clock scheme for the TPG and the clock tree feeding the TPG. Numerous advantages can be found in applying such a technique. The fault coverage and the test time are roughly the same as those achieved using a standard BIST scheme. The area overhead is nearly negligible and there is no penalty on the circuit delay. The proposed BIST scheme does not require any circuit design modification beyond the parallel BIST technique, is easily implemented and has low impact on the design time. It has been implemented based on an LFSR-based TPG, but can also be designed using a cellular automata. Reductions of the energy, average power and peak power consumption during test operation are up to 94%, 55% and 48% respectively for ISCAS and MCNC benchmark circuits.*

**List of keywords :** Parallel BIST, Low-power Design, Test & Low Power, Low Power BIST  
**Suggested topic:** Built-in Self-Test (BIST)

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**Abstract:** *In this paper, we present a new low power test-per-clock BIST test pattern generator that provides test vectors which can reduce the switching activity during test operation. The proposed low power/energy BIST technique is based on a modified clock scheme for the TPG and the clock tree feeding the TPG. Numerous advantages can be found in applying such a technique.*

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## 1. Introduction

Low Power consumption has become increasingly important in hand-held communication systems and battery operated equipment, such as laptop computers, audio and video-based multimedia products, and cellular phones. For this new class of battery-powered devices, the energy consumption is a critical design concern since it determines the lifetime of the batteries. In addition, the capabilities presented by advanced submicron CMOS technology allowing to put millions on transistors on chip and clocking at hundreds of MHz have compounded the problem of power/energy consumption. A strong push towards reducing power consumption is also coming from producers of high-end systems. The cost associated with packaging and cooling of such devices is huge and technological constraints are severe: unless power consumption is reduced, the resulting heat limits systems performance [1].

Intensive research efforts have been devoted to develop algorithmic and technological solutions for reducing power consumption during *normal* circuit operation [1]; they are not concerned with power consumption minimization during *test* operation. The main motivation for considering power consumption during test operation is that power and energy of a digital system are considerably higher in test mode than in system mode [2,3,4]. It has been shown in [2] that the power consumption during test can be as high as 200% of the power consumed in the normal mode. The reason for this increased power consumption is that test patterns cause as many nodes switching as possible while a power saving system mode only activates a few modules at the same time. Another reason is that successive functional input vectors applied to a given circuit during system mode have a significant correlation, while the correlation between consecutive test patterns (produced by an LFSR for example) may be very low [5].

This elevated switching activity during test may be responsible for cost, reliability, performance verification, autonomy and technology related problems. A survey of these problems is given in [6]. For example, in battery-powered devices, the power consumed

during application of power-up or periodical on-line tests, which are often implemented resorting to the Built-In Self Test (BIST) approach, can dramatically shorten the battery lifetime. Another example of such problems is that increased circuit activity and hence power/energy consumption leads to increased current flows during test, making the use of expensive packages for the removal of excessive heat an imperative need. Increased heat leads also to serious silicon failure mechanisms, such as electromigration [7], that reduce the reliability of a system operating under such conditions. Power consumption during BIST is also a major concern in manufacturing testing [2]. BIST is usually executed at system clock rate and its execution typically results in considerably high circuit activity. If BIST is activated when the device is fully packaged, the power consumption may overpass the device package limits and lead to circuit destruction. This problem is even more critical when testing current System-on-Chip (SOC) designs since many IP (Intellectual Property) cores are tested in parallel within the same BIST session, causing considerably high circuit activity [8].

Recently, techniques to cope with the power and energy problems during BIST have appeared. A brief overview of these techniques is given in Section 2. In this paper, we address the low power testing problem in BIST. BIST is well known for its numerous advantages such as improved testability, at-clock-speed test of modules, reduced need for automatic test equipment, and support during system maintenance [9,10]. Moreover, with the emergence of core-based SOC designs, BIST represents one of the most favorable testing method since it allows to preserve the intellectual property of the design. In most complex SOC designs characterized by very poor controllability and observability, BIST is even probably the only practical solution for efficient testing [8].

In this work, we adopt a test-per-clock BIST architecture where a modified Linear Feedback Shift Register (LFSR) is used as Test Pattern Generator (TPG) to generate low power vectors. The proposed low power/energy BIST technique is based on a gated clock scheme for the TPG and the clock tree feeding the TPG. More specifically, a clock whose speed is half of the normal speed is used to activate one half of the D flip-flops in the modified LFSR during one clock cycle of the test session. During the next clock cycle, the second half of the D flip-flops is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with the master clock and have the same but shifted in time period. This scheme is used too for the clock tree feeding the TPG. The use of such a modified clock scheme lowers the transition density in both the Circuit Under Test (CUT), the TPG and the clock tree feeding the TPG. Reduction in power consumption during BIST comes from the reduction of the switching activity in both parts. Compared with existing low power BIST techniques, our solution offers a number of advantages. The fault coverage and the test time, which are among the main constraints, are roughly the same as those achieved with a standard BIST scheme. The area overhead is negligible and there is no penalty on the circuit delay (which is also an important parameter). The proposed BIST scheme does not require any circuit design modification beyond standard BIST techniques and is very easy to implement (low impact on the design time). It has been implemented based on an LFSR-based TPG but can also be designed using a cellular automata. Reductions of the energy, average power and peak power consumption during test are up to 94%, 55% and 48% respectively for ISCAS and MCNC benchmark circuits.

The remainder of the paper is organized as follows. In the next section, we first discuss the energy and power modeling. Next, we review the existing techniques that cope with the power and energy problems during BIST. In Section 3, we first detail the basic idea of the proposed low power BIST scheme. Next, we present the modified LFSR used as TPG. Section 4 is devoted to the description of the complete BIST TPG architecture. The simulation results

obtained from the ISCAS and MCNC benchmark circuits are reported in Section 5. Concluding remarks are given in Section 6.

## 2. Background and related work

### 2.1 Energy and power modeling

Three parameters are important for evaluating the power properties of a BIST architecture:

- The consumed *energy* directly corresponds to the switching activity generated in the circuit during test application, and has impact on the battery lifetime during remote testing.
- The *average power* consumption is given by the ratio between the energy and the test time. This parameter is even more important than the energy as hot spots and reliability problems may be caused by constantly high power consumption.
- The *peak power* consumption corresponds to the highest switching activity generated in the CUT during one clock cycle. The peak power determines the thermal and electrical limits of components and the system packaging requirements [1]. If the peak power exceeds certain limits, the correct functioning of the circuit is no longer guaranteed.

For the reader's convenience, we recall in the following the equations that are normally adopted to model power and energy dissipated by a CMOS device.

Power consumption in CMOS circuits can be classified into static and dynamic. Static power dissipation is due to leakage current or other current drawn continuously from the power supply. Dynamic dissipation is due to (i) short circuit current and (ii) charging and discharging of load capacitances during output switchings. For the current CMOS technology, dynamic power is the dominant source of power consumption, although this may change for future developments of high scaled integration [11]. The average energy consumed at node  $i$  per switching is  $\frac{1}{2}C_iV_{DD}^2$  where  $C_i$  is the equivalent output capacitance and  $V_{DD}$  the power supply voltage [12]. Therefore, a good approximation of the energy consumed in a period is  $\frac{1}{2}C_i s_i V_{DD}^2$  where  $s_i$  is the number of switchings during the period. Nodes connected to more than one gate are nodes with higher parasitic capacitance. Based on this fact, and in a first approximation, capacitance  $C_i$  is assumed to be proportional to the fanout of the node  $F_i$  [13]. Therefore, an estimation of the energy  $E_i$  consumed at node  $i$  during one clock period is:

$$E_i = \frac{1}{2} \cdot s_i \cdot F_i \cdot c_0 \cdot V_{DD}^2$$

where  $c_0$  is the minimum size parasitic capacitance of the circuit. According to this expression, the estimation of the energy consumption at the logic level requires the calculation of the fanout  $F_i$  and the number of switchings on node  $i$ ,  $s_i$ . The fanout of the nodes is defined by circuit topology, and the switchings can be estimated by a logic simulator (note that in a CMOS circuit, the number of switchings is calculated from the moment the input vector is changed until the moment the internal nodes reach the new stable state, including the hazard switching). The product  $s_i F_i$  is named Weighted Switching Activity (WSA) of node  $i$  and represents the only variable part in the energy consumed at node  $i$  during test application. According to the above formulation, the energy consumed in the circuit after application of a pair of successive input vectors  $(V_{k-1}, V_k)$  can then be expressed by:

$$E_{V_k} = \frac{1}{2} \cdot c_0 \cdot V_{DD}^2 \cdot \sum_i s(i,k) \cdot F_i$$

where  $i$  ranges all the nodes of the circuit and  $s(i,k)$  is the number of switchings provoked by  $V_k$  at node  $i$ . Consider now a pseudo-random test sequence of length  $Length_{rest}$ , where

$Length_{test}$  is the test length required to achieve the targeted fault coverage, the total energy consumed in the circuit during application of the complete test sequence is:

$$E_{total} = \frac{1}{2} \cdot c_0 \cdot V_{DD}^2 \cdot \sum_{V_k} \sum_i s(i,k) \cdot F_i$$

Let us denote the clock period as  $T$ . By definition, the instantaneous power is the power consumed during one clock period. Therefore, the instantaneous power consumed in the circuit after application of vectors  $(V_{k-1}, V_k)$  can be expressed as follows:

$$P_{inst}(V_k) = \frac{E_{V_k}}{T}$$

The peak power consumption corresponds to the maximum of the instantaneous power consumed during the test session. Therefore, it corresponds to the highest energy consumed during one clock period, divided by  $T$ . More formally, it can be expressed as follows:

$$P_{peak} = \max_k P_{inst}(V_k) = \frac{\max_k (E_{V_k})}{T}$$

Finally, the average power consumed during the test session is the total energy divided by the test time, and is given as follows:

$$P_{ave} = \frac{E_{total}}{Length_{test} \cdot T}$$

According to the above expressions of the power and energy consumption, and assuming a given CMOS technology and supply voltage for the circuit design, the number of switchings  $s_i$  of a node  $i$  in the circuit is the only parameter that has impact on both the energy, the peak power and the average power consumption. Consequently, low power BIST solutions that target switching activity reduction during test are preferable.

## 2.2 Related work

While academic research on Low Power Design and on BIST has been performed nearly independently, the industrial practice has required ad hoc solutions for considering power consumption during BIST [14]. Practiced solutions include:

- Oversizing power supply, package and cooling to stand the increased current during testing. Breaks are inserted into the test process for avoiding hot spots.
- Test with reduced operation frequency.

The first solution increases both hardware costs and test application time. The second proposal uses less hardware, but the reduced system frequency increases test application time and may lead to a loss of defect coverage as dynamic faults may be masked. Moreover, this solution reduces the power consumption at the expense of a longer test time, but does not reduce the total energy consumption during test, important for the lifetime of the battery.

The industrial needs initiated academic research. Hence, techniques to cope with the power and energy problems during BIST have appeared recently. These approaches targeting combinational circuits can be classified as follows:

1) *Distributed BIST Control Schemes* [2,15]. The goal in these approaches is to determine the BISTed blocks of a complex design to be activated in parallel at each stage of the test session in order to reduce the number of concurrently tested modules. The average power is reduced and consequently, the temperature related problems avoided by the increase of the test time duration. On the other hand, the total energy remains constant and the autonomy of the system is not increased.

2) *Vector Filtering Architectures* [16,17,18]. As each vector applied to the CUT consumes power but not every vector generated by the pseudo-random TPG contributes to the final fault coverage, the vector filtering architectures consist in preventing application of non-detecting vectors to the CUT. This approach is very effective in reducing power without reducing fault coverage, but does not preserve the CUT from excessive peak power consumption and can lead to high area overhead.

3) *Low Power Test Pattern Generators* [5,19,20,21]. TPGs based either on LFSRs or Cellular Automata (CA) are carefully designed to reduce the activity at circuit inputs, thus reducing power consumption. These approaches effectively reduce power during test but sometimes at a cost of sub-optimal fault coverage and with no reduction of the peak power consumption.

4) *Circuit Partitioning for Low Power BIST* [22]. This approach consists in partitioning the original circuit into structural sub-circuits so that each sub-circuit can be successively tested through different BIST sessions. In partitioning the circuit and planning the test session, the average power, the peak power and the energy consumption during BIST are minimized at a low expense in terms of area overhead and with no loss of fault coverage. The only drawback of this approach is that it requires circuit design modification.

The above mentioned approaches can be easily adapted for testing sequential circuits through customized full-scan architectures [23,24].

### **3. Gated clock scheme for generating low power vectors**

#### *3.1 Basic idea*

The reduction of the power consumption in a test-per-clock BIST environment is commonly achieved by reducing the switching activity in the CUT. Furthermore, it has been demonstrated in [5] that the switching activity in a time interval (*i.e.* the average power) dissipated in a CUT during BIST is proportional to the transition density at the circuit inputs. Thereby, several low power test pattern generators have been proposed to reduce the activity at circuit inputs (see above description in part 2.2). Among these techniques, the DS-LFSR proposed in [5] consists in using two LFSRs, a slow LFSR and a normal speed LFSR, as TPG. Inputs driven by the slow LFSR are those which may cause more transitions in the circuit. Although this technique reduces the average power consumption while maintaining a good fault coverage level, the peak power consumption cannot be reduced in practice (a full bit changing may occur at circuit inputs every  $d$  clock cycles where  $d = \text{normal clock speed} / \text{slow clock speed}$ ). This point represents a severe limitation of the method as the peak power consumption is a critical parameter that determines the electrical limits of the circuit and the packaging requirements.

As in [5], the low power/energy BIST technique proposed in this paper is based on a modified clock scheme for the pseudo-random TPG. Basically, a clock whose speed is half of the normal speed is used to activate one half of the D flip-flops in the TPG (*i.e.* a modified LFSR) during one clock cycle. During the next clock cycle, the second half of the D flip-flops is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with a master clock CLK and have the same but shifted in time period. The clock CLK is the clock of the circuit in the normal mode and has a period equal to  $T$ . The basic scheme of the proposed low power test pattern generator with the corresponding clock waveforms are depicted in Figure 1. As one can observe, a test vector is applied to the CUT at each clock cycle of the test session. However, only one half of the circuit inputs can be

activated during this time. Consequently, the switching activity in a time interval (*i.e.* the average power) as well as the peak power consumed in the CUT are minimized. Moreover, the power consumed in the TPG is also minimized since only one half of the D flip-flops in the TPG can be activated in a given time interval. Another important feature of the proposed solution is that the total energy consumption during BIST is reduced since the test length produced by the modified LFSR is roughly the same than the test length produced by a conventional LFSR-based TPG to reach the same or sometimes a better fault coverage. Results are given in Section 5 to highlight this point.

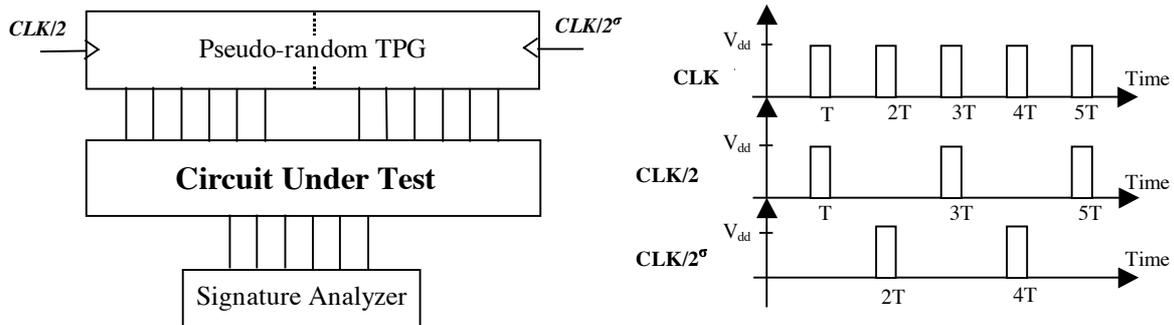


Figure 1: Basic scheme of the low power test pattern generator

### 3.2 The low power TPG

The idea behind the use of such a low power TPG is to reduce the number of transitions on primary inputs at each clock cycle of the test session, hence reducing the overall switching activity generated in the CUT. Let us consider a CUT with  $n$  primary inputs. A  $n$ -stage primitive polynomial LFSR with a clock CLK would be used in a conventional pseudo-random BIST scheme. Here, we use a modified LFSR composed of  $n$  D-type flip-flops and two clocks  $CLK/2$  and  $CLK/2^\sigma$ , and constructed as depicted in Figure 2 ( $n=6$  in the example of Figure 2). As one can observe, this modified LFSR is actually a combination of two  $n/2$ -stage primitive polynomial LFSRs, each of them being driven by a single clock  $CLK/2$  or  $CLK/2^\sigma$ . The D cells belonging to the first LFSR (referred to as LFSR-1 in the sequel) are interleaved with the cells of the second LFSR (referred to as LFSR-2 in the sequel), thus allowing to better distribute the signal activity at the inputs of the CUT.

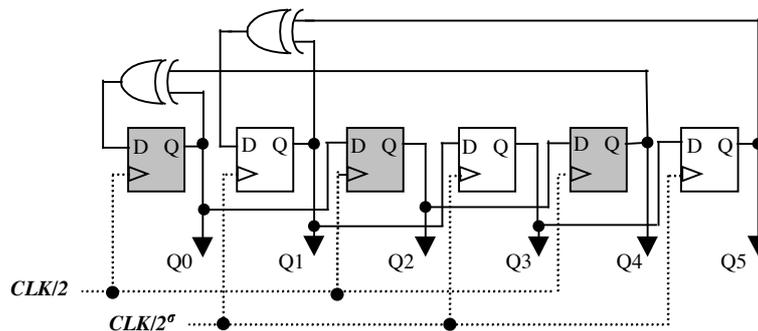


Figure 2: An example of the modified LFSR TPG

In order to better describe the functioning of the low power TPG, the timing diagram of the test sequence generated by the example TPG shown in Figure 2 is reported in Table 1. Assume that the seed  $\langle 001 \rangle$  has been chosen for both LFSRs, such that the first vector applied to the CUT at time T is  $\langle 100001 \rangle$ . Only LFSR-1 is active during the first clock cycle (LFSR-2 is in stand-by mode). This is illustrated in the two last columns of Table 1 in which a

grey cell represents the active LFSR in the corresponding clock cycle. During the next clock cycle, LFSR-2 is active (LFSR-1 is in stand-by mode) and vector <110000> is applied to the CUT.

The advantage of the modified LFSR composed of two interleaved  $n/2$ -stage LFSRs (over a simpler structure composed of two separated  $n/2$ -stage LFSRs) is that it allows to better distribute the signal activity at the circuit inputs during the BIST session. This is particularly important for circuits in which the input cones of the primary outputs are highly non-overlapping. In this case, two separated LFSRs would activate only one part of the circuit in a given time interval, instead of the whole circuit with the proposed structure in which two LFSRs are interleaved. Shorter test lengths to reach a target fault coverage can hence be predicted with the proposed interleaved LFSR structure.

Time	Q0	Q1	Q2	Q3	Q4	Q5	LFSR-1	LFSR-2
0	0	0	0	0	1	1		
T	<b>1</b>	0	<b>0</b>	0	<b>0</b>	1		
2T	1	<b>1</b>	0	<b>0</b>	0	<b>0</b>		
3T	<b>1</b>	1	<b>1</b>	0	<b>0</b>	0		
4T	1	<b>1</b>	1	<b>1</b>	0	<b>0</b>		
5T	<b>1</b>	1	<b>1</b>	1	<b>1</b>	0		
6T	1	<b>1</b>	1	<b>1</b>	1	<b>1</b>		
7T	<b>0</b>	1	<b>1</b>	1	<b>1</b>	1		
8T	0	<b>0</b>	1	<b>1</b>	1	<b>1</b>		

Table 1: Timing diagram of the test sequence generated by the TPG shown in Figure 2

Two additional comments about the above structure are now given. Firstly, in the case where the number of circuit inputs  $n$  is odd, the two interleaved LFSRs are as follows: LFSR-1 is composed of  $n/2+1$  D-type flip-flops while LFSR-2 is a  $n/2$ -stage primitive polynomial LFSR. Not any change in the operating mode of the low power TPG is involved in this case. Secondly, the same low power TPG can be built if a CA is preferred to an LFSR. In this case, the two  $n/2$ -stage LFSRs are replaced by two CA of the same size.

#### 4. Complete BIST TPG structure

The complete BIST TPG structure proposed in this paper is depicted in Figure 3.

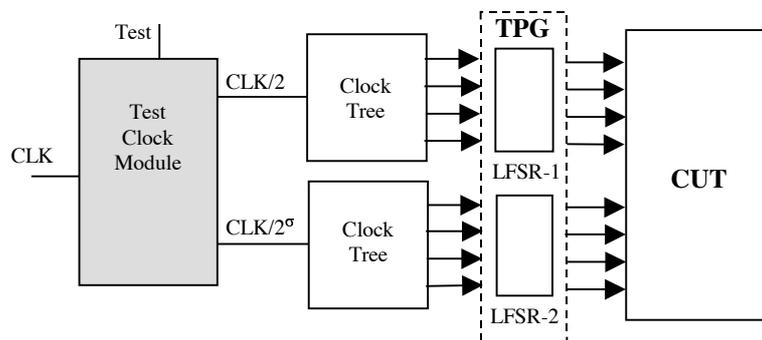


Figure 3: The complete BIST TPG structure

This structure is first composed of a test clock module which provides test clock signals  $CLK/2$  and  $CLK/2^\sigma$  from the master clock  $CLK$  used in the normal mode. The signal “Test” allows to switch from the test mode ( $=0$ ) to the normal mode. As two different clock speeds are needed for the TPG, two clock trees are used in our proposed BIST scheme rather than a single one. These clock trees are carefully designed so as to correctly balance the clock signals

feeding each part of the modified LFSR. Finally, the main part of the TPG (*i.e.* the modified LFSR) is connected to the CUT.

The test clock module which provides test clock signals  $CLK/2$  and  $CLK/2^\sigma$  from the master clock  $CLK$  is given in Figure 4. This module is formed by a simple feedback of a D-type flip-flop and four logic gates, and allows to generate non-overlapping test clock signals as those represented in Figure 1. This structure is very simple and requires a small overhead of hardware. Moreover, it is designed with minimum impact on performance and timing. In fact, some of the already existing driving buffers of the clock tree have to be transformed into AND gates as seen in Figure 4. These gates mask each second phase of the fast system (or test) clock. All the other hardware of the complete BIST TPG structure is outside the clock tree as depicted in Figure 4.

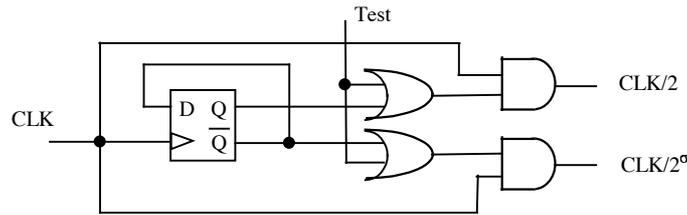


Figure 4: The test clock module

As two different clock signals are used by the TPG, the clock tree feeding the D flip-flops has to be modified. In the proposed BIST TPG structure, two clock trees are therefore implemented, each of them with a clock speed which is half of the normal speed ( $CLK/2$  and  $CLK/2^\sigma$ ). These clock trees have to be carefully designed so as to correctly balance the clock signals feeding the D flip-flops in both the normal mode and the test mode. Let us consider again the example TPG shown in Figure 2. The corresponding clock trees in the test mode are depicted in Figure 5.a given below. Each of them has a fanout of 3 and is composed of a single buffer. During the normal mode of operation, the clock tree feeding the input register at the normal speed can therefore be easily reconstructed as shown in Figure 5.b. Note that using two clock trees driven by a slower clock (rather than a single one) allows to further reduce the power consumption during BIST significantly. Since the clock tree usually requires a significant amount of power in a system, this reduction cannot be obtained by the standard techniques targeting only the CUT and the TPG.

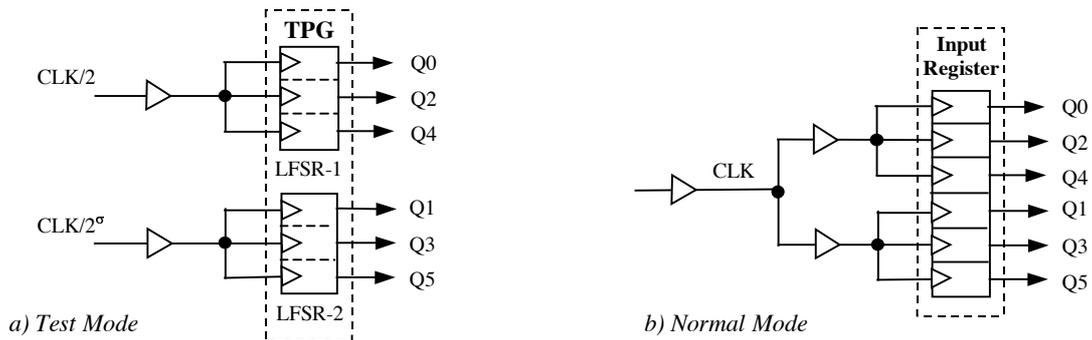


Figure 5: The clock tree in the test mode and in the normal mode

The use of such a TPG structure for generating stuck-at fault test vectors in pseudo-random BIST lowers the transition density in both the combinational CUT, the modified LFSR and the clock tree feeding the LFSR. Reduction in power consumption during BIST comes from the reduction of the switching activity in all the parts. Compared with existing low power test pattern generators, our solution offers a number of advantages. The fault coverage and the test

time are the same as those achieved with a standard BIST scheme. The area overhead, which is due to the test clock module and the modified LFSR, is negligible. The proposed BIST scheme does not require any further circuit design modification and is very easy to implement. It therefore has a low impact on the system design time and has nearly no penalty on the circuit delay.

## 5. Experimental results

The benchmarking process described here was performed on some circuits of the ISCAS'85 [25], MCNC'93 [26], and ISCAS'89 (full scan version) [27] benchmark suites on a Sun Enterprise 3000 with 256 MB of RAM. The goal of the experiments we performed has been first to make sure that the main test parameters (test length and fault coverage) keep the same values under the new low power BIST scheme, and next to measure the power and energy savings that our solution allows to obtain on the CUT, the TPG and the clock tree.

First, results of the proposed low power BIST technique in terms of test length and fault coverage are reported in Table 2. All experiments are based on pseudo-random pattern testing, and complete fault coverage cannot be expected for each circuit. The first part of Table 2 shows the test length and the fault coverage obtained from a classical LFSR as TPG. This information is listed in the second and third columns. In the second part of Table 2, the same results (test length and fault coverage) obtained with the proposed low power TPG are given for each benchmark circuit. The polynomials for all the LFSRs were chosen from a set of primitive polynomials under the constraint to provide the highest fault coverage. The seed for these LFSRs was calculated from the random-based procedure described in [28] which provides the smallest value of the product (test length  $\times$  switching activity) for a target fault coverage. Fault coverage calculations were performed with TestGen of Synopsys [29].

Circuit	Standard BIST		Low Power BIST	
	Test length	FC (%)	Test length	FC (%)
seq	9 985	77.15	9 076	77.15
apex6	9 501	97.75	8 469	97.80
apex3	6 624	100	7 249	100
apex1	9 988	97.97	9 644	97.62
alu4	9 847	90.15	9 874	88.14
c6288	78	99.56	87	99.56
c7552	9 700	94.08	8 491	94.08
s1423	9 961	98.49	8 311	98.87
s9234	9 590	83.43	9 402	83.56
s13207	9 974	90.90	9 942	92.40
s15850	9 796	90.81	9 533	90.61
s38417	9 943	91.66	9 601	91.75
s38584	9 929	94.24	9 645	94.10

Table 2: Test length and fault coverage comparison

Regarding the above results, it should be noted that the fault coverage obtained with a standard BIST scheme is not affected by the proposed low power BIST scheme. The fault coverage is roughly the same as that obtained with a classical LFSR, with a test length which is most of the time decreased compared with the test length in a standard BIST scheme.

Now, results about the power and energy savings achieved by the proposed low power BIST scheme are discussed. Power consumption in each circuit was estimated by using PowerMill,

a dynamic simulator provided by the Epic Technology Group of Synopsys [30], assuming a clock period of 60 nanoseconds (frequency equal to 16.6 MHz) and a power supply voltage of 5V. Experiments performed on each circuit have been done with technology parameters extracted from the HSPICE level 6 foundry model for a 0.8 $\mu$ m digital CMOS process. Results of the power savings in the CUT are summarized in Table 3 for the benchmark circuits. For each circuit, we have reported the peak power, the average power, and the energy obtained, first with a classical LFSR as TPG (first part of Table 3) and next with the proposed low power TPG. Peak power and average power are expressed in milliWatts. Concerning energy, the values reported were obtained by performing the product between the average power and the test time (length $\times$ T). Energy is expressed in microJoules. The last part in Table 3 shows the reductions in peak power, average power and energy consumption expressed in percentages. These results on benchmark circuits show that average power reduction of up to 55 %, peak power reduction of up to 48 %, and energy reduction of up to 94 % can be achieved by using the proposed low power BIST scheme compared to a standard BIST scheme in which a conventional LFSR is used as TPG.

Circuit	Standard BIST			Low Power BIST					
	peak [mW]	power [mW]	energy [ $\mu$ J]	peak [mW]	power [mW]	energy [ $\mu$ J]	peak reduct	power reduct	energy reduct
seq	1080	13.7	8.2	810	7.9	0.46	25 %	42 %	94 %
apex6	845	6.35	3.62	434.5	3.63	1.84	48 %	42 %	49 %
apex3	474	6.2	2.46	345	3.88	1.68	20 %	37 %	31 %
apex1	530	5.05	3.02	371.5	3.36	1.94	30 %	33 %	35 %
alu4	1000	21.7	12.8	700	11.55	6.84	30 %	46 %	46 %
c6288	1595	116	0.54	1275	98	0.51	20 %	15 %	5 %
c7552	2815	55.8	32.4	2380	35.5	18.08	15 %	36 %	44 %
s1423	595	7.8	4.66	313.5	3.5	1.74	47 %	55 %	62 %
s9234	2350	42.4	24.4	1405	25.1	14.1	40 %	40 %	42 %
s13207	3285	57.5	34.4	1830	29.9	17.8	44 %	48 %	48 %
s15850	3545	77	45.25	1875	43.05	24.6	47 %	44 %	45 %
s38584	11950	214.5	127.8	6700	118	68.2	44 %	45 %	46 %

Table 3: Power and energy savings in the CUT

Although the power consumed in the TPG is normally lower than the power consumed in the CUT, it is not negligible. Moreover, reducing the power in the TPG can be attractive when testing circuits with a high number of inputs. In this case, the number of D flip-flops in the LFSR or in the modified LFSR is significant (remember that we assume a test-per-clock BIST scheme), and the power consumed in these flip-flops may represent a significant portion of the total power/energy consumption.

In order to first measure the power consumed in the flip-flops of the TPG and next evaluate the efficiency of our proposed technique in reducing the power in the TPG, we performed another set of experiments. The same electrical and technological parameters than those utilized to evaluate the power savings in the CUT were used. Results are reported in Table 4 for benchmark circuits which have a high number of inputs. As can be seen, the power and energy consumed in the flip-flops is always significant compared with the power and energy consumed in the CUT. Therefore, reducing the power in the TPG is really important for this kind of circuits. On the other hand, the above results show that our low power BIST technique reduces by more than half the average power and the energy consumed in the TPG (compared with a standard BIST scheme). As we cannot handle sequential logic elements such as D flip-flops with our version of PowerMill [30], the evaluation of the average power consumed in the TPG was performed from an estimated value of the power consumed in each flip-flop

during BIST. This estimated value has been calculated by using HSPICE and by counting the average number of transitions in a D flip-flop during one clock cycle of the test session. The peak power consumption has not been evaluated.

Circuit	#inputs	#gates (GE)	Standard BIST		Low Power BIST			
			power [mW]	energy [ $\mu$ J]	power [mW]	energy [ $\mu$ J]	power reduct	energy reduct
c7552	206	3315	26.7	15.5	11.1	5.6	58.4 %	63.8 %
s9234	247	4678.5	32.25	18.5	13.3	7.5	58.7 %	59.4 %
s13207	700	6395.5	91.65	54.8	37.9	22.6	58.6 %	58.7 %
s15850	611	7987	79.5	46.7	33	18.8	58.4 %	59.7 %
s38417	1664	18204	215	128.2	97.2	55.9	54.7 %	56.3 %
s38584	1464	20446.5	191.1	113.8	79.2	45.8	58.5 %	59.7 %

Table 4: Power and energy savings in the TPG

Reducing the power/energy consumption in the clock tree is an important issue since it represents a significant portion of the total energy consumed during BIST [23]. The proposed low power BIST scheme reduces the switching activity in the clock tree as illustrated in the previous section. In order to evaluate the saving in power and energy consumption in the clock tree, we performed a new set of experiments. The same electrical and technological parameters as those utilized to evaluate the power savings in the CUT were used. Results are reported in Table 5 for some of the biggest benchmark circuits. These results are based on a simple clock tree design with one buffer (or inverter) feeding 4 buffers in the next level. Note that this value is important from a design point of view but is not really important in our evaluations which have a comparison purpose. Actually, another value of the fanout would provide different intrinsic values of the power and energy (a higher value of the fanout would lead to lower values of the power and energy consumed in the clock trees), but would provide approximately the same ratio between power in the low power BIST scheme and power in a standard BIST scheme compared with those presented in Table 5.

Circuit	Standard BIST			Low Power BIST					
	peak [mW]	power [mW]	energy [ $\mu$ J]	peak [mW]	power [mW]	energy [ $\mu$ J]	peak reduct	power reduct	energy reduct
c6288	169	1.1	0.005	77.5	0.5	0.002	54 %	54 %	60 %
c7552	875	7	4.07	409	3.1	1.57	53 %	55 %	61 %
s9234	1220	8.1	4.66	505	3.5	1.97	58 %	56 %	57 %
s13207	2920	27.8	16.6	1395	11.1	6.62	52 %	60 %	60 %
s15850	2190	18	10.6	1320	10.5	6.0	39 %	41 %	43 %
s38417	7900	62.5	37.2	3660	34.2	19.7	53 %	45 %	47 %
s38584	5250	54	32.1	2930	21.3	12.3	44 %	60 %	61 %

Table 5: Power and energy savings in the clock tree

These results on benchmark circuits show that average power reduction of up to 60 %, peak power reduction of up to 58 %, and energy reduction of up to 61 % can be achieved in the clock tree by using the proposed low power BIST scheme. These percentages are evaluated in comparison with a standard BIST scheme in which a single clock speed is used.

Table 5 compares the power consumed in the clock tree for standard BIST and our approach, and we argue that the actual layout of the clock tree has little impact as the ratio between both will be independent. On the other hand, people are also interested in the overall power reduction on the circuit. Unfortunately, evaluating this overall power reduction is difficult since the real layout is needed for this. A possible approximate solution would be to sum up

Tables 3, 4, and 5 given above. But in this case, the ratio mentioned would be incorrect as clock lines are usually longer and often even wider than the electrical signal lines, and have more capacity. Hence the clock is actually weighted higher (experience is about 40 % energy in the clock trees). This effect is in favor of our approach (we receive significant reduction for the clock tree), but is difficult to quantify at higher design levels. For this reason, we do not present overall results based on the summation of Tables 3, 4, and 5 given above.

## 6. Conclusion

A TPG for test-per-clock BIST that generates low power vectors which can reduce switching activity during test application is proposed in this paper. The proposed low power/energy BIST technique is based on a modified clock scheme for the TPG and the clock tree feeding the TPG. The use of such a modified clock scheme lowers the transition density in both the Circuit Under Test (CUT), the TPG and the clock tree feeding the TPG. Reduction in power consumption during BIST comes from the reduction of the switching activity in both parts. Compared with existing low power BIST techniques, our solution offers a number of advantages. The fault coverage and the test time are roughly the same as those achieved with a standard BIST scheme. The area overhead is negligible and there is no penalty on the circuit delay. The proposed BIST scheme does not require any circuit design modification beyond standard BIST is very easy to implement and has low impact on the design time. It has been implemented from an LFSR-based TPG in our work but can also be designed from a cellular automata. Reductions of the energy, average power and peak power consumption during test operation are up to 94%, 55% and 48% respectively for ISCAS and MCNC circuits.

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