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Abstract: Small gate delay faults (SDFs) are not detectable at-speed, if they can only be propagated along short paths. These hidden delay faults (HDFs) do not influence the circuit's behavior initially, but they may indicate design marginalities leading to early-life failures, and therefore they cannot be neglected. HDFs can be detected by faster-than-at-speed test (FAST), where typically several different frequencies are used to maximize the coverage. A given set of test patterns P potentially detects a HDF if it contains a test pattern sensitizing a path through the fault site, and the efficiency of FAST can be measured as the ratio of actually detected HDFs to potentially detected HDFs. The paper at hand targets maximum test efficiency with a minimum number of frequencies. The procedure starts with a test set for transition delay faults and a set of preselected equidistant frequencies. Timing-accurate simulation of this initial setup identifies the hard-to-detect faults, which are then targeted by a more complex timing-aware ATPG procedure. For the yet undetected HDFs, a minimum number of frequencies are determined using an efficient hypergraph algorithm. Experimental results show that with this approach, the number of test frequencies required for maximum test efficiency can be reduced considerably. Furthermore, test set inflation is limited as timing-aware ATPG is only used for a small subset of HDFs.

Preprint

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Optimized Selection of Frequencies for Faster-than-at-Speed Test

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Abstract— Small gate delay faults (SDFs) are not detectable at-speed, if they can only be propagated along short paths. These hidden delay faults (HDFs) do not influence the circuit’s behavior initially, but they may indicate design marginalities leading to early-life failures, and therefore they cannot be neglected. HDFs can be detected by faster-than-at-speed test (FAST), where typically several different frequencies are used to maximize the coverage. A given set of test patterns P potentially detects a HDF if it contains a test pattern sensitizing a path through the fault site, and the efficiency of FAST can be measured as the ratio of actually detected HDFs to potentially detected HDFs.

The paper at hand targets maximum test efficiency with a minimum number of frequencies. The procedure starts with a test set for transition delay faults and a set of preselected equidistant frequencies. Timing-accurate simulation of this initial setup identifies the hard-to-detect faults, which are then targeted by a more complex timing-aware ATPG procedure. For the yet undetected HDFs, a minimum number of frequencies are determined using an efficient hypergraph algorithm.

Experimental results show that with this approach, the number of test frequencies required for maximum test efficiency can be reduced considerably. Furthermore, test set inflation is limited as timing-aware ATPG is only used for a small subset of HDFs.

I. INTRODUCTION

Hidden delay faults (HDFs) are small gate delay faults for which even the slack of the longest sensitizable path is too large to observe the fault effect at nominal (at-speed) frequency. Consequently, HDFs are immune to timing-aware ATPG and cannot even be detected by at-speed testing. Although they are not visible during normal operation and will not be observed in the field, they may point to design marginalities, and thus to potential early-life failures (ELFs) [Kim10]. Therefore, it is important to screen out as many HDFs as possible already during manufacturing test. Faster-than-at-speed test (FAST) addresses this problem by applying the test patterns with frequencies above the nominal system frequency [Yan03]. To maximize the HDF coverage, in general, several different frequencies distributed over the interval $[f_{nom}, f_{max}]$ are required, where f_{max} is the highest frequency during test and f_{nom} denotes the nominal test frequency.

The maximal frequency f_{max} depends on the capabilities of the automatic test equipment (ATE) or the on-chip clock gen-

erators [McLaurin00, Press06, Tayade08, Pei10]. Typically f_{max} is up to 3 times higher than the nominal clock rate [Amodeo05, Ahmed06, Lee08]. For the selection of intermediate frequencies mainly two strategies have been followed so far. The first strategy simply uses a preselected set F of equidistant frequencies in $[f_{nom}, f_{max}]$, e.g. $1.5 \cdot f_{nom}$, $2 \cdot f_{nom}$, $2.5 \cdot f_{nom}$, and $3 \cdot f_{nom} = f_{max}$, and tries to adjust the test set appropriately. Here, basic schemes sample each pattern for multiple frequencies [Yan03, Lee08], while more sophisticated approaches select or generate patterns specifically for each frequency [Krusemann04, Ahmed06, Yoneda11, Fu12]. In contrast to that, the second strategy works with a given set of test patterns P and determines a minimum set of frequencies, such that maximum *test efficiency* is achieved, i.e. all HDFs can be detected whose associated transition faults are covered by P [Hellebrand14].

Working with a set F of preselected equidistant frequencies can facilitate clock generation, but the number of test patterns may increase considerably. Furthermore, complete HDF coverage cannot be guaranteed, as some faults may become visible only with specific frequencies outside F . On the other hand, optimizing frequencies with respect to a given test set P provides the best possible HDF coverage achievable with P and technically feasible frequencies not exceeding f_{max} . This supports low cost test generation, and the results in [Hellebrand14] indicate that typically a small number of frequencies can provide maximum test efficiency. However, these results have only been verified with symbolic simulation and may be too optimistic. Furthermore, the computational effort for solving the underlying optimization problem may grow very high for larger circuits.

This paper presents a new hybrid approach for selecting FAST frequencies, which combines the advantages of both previous strategies. To the best of our knowledge, it is the first approach that achieves the following goals at the same time:

- maximum test efficiency possible with frequencies not exceeding f_{max} ,
- verification by exact timing-aware fault simulation,
- minimum number of frequencies.

Moreover, it limits the test size and keeps the computational effort low. The procedure starts with a test set for transition

faults and a preselected set of equidistant frequencies. Additional timing-aware patterns are then generated only for the remaining hard-to-detect faults, and optimal frequency selection is based on the complete test set combining the patterns for transition test with the timing-aware patterns.

The remainder of this paper is organized as follows. Section II introduces the terminology and summarizes the necessary background. Subsequently, the new approach for frequency selection is explained in detail in Sections III and IV. Section V demonstrates its effectiveness with the help of experimental data, and finally, Section V concludes the paper.

II. BACKGROUND

This section provides the necessary background and the terminology to understand the proposed approach for selecting FAST frequencies.

A. Detection Ranges and Frequency Selection

This paper assumes a gate being faulty, if its delay exceeds 3σ , where σ is the standard deviation of the gate delay. Depending on the test set and the test frequency, such a fault can be a hidden fault as specified in Definition 1.

Definition 1: Let φ be a gate delay fault, P a set of test patterns, and let f be a frequency. If φ is not detected by P at frequency f , then φ is called a *hidden delay fault with respect to P and f* .

To clearly show under which conditions a small delay fault is a hidden delay fault, the set of all hidden delay faults with respect to a test set P and a set of frequencies F is denoted by $\Phi(P, F)$.

Frequencies f are associated with observation times $t = 1/f$, assuming that the test response is sampled at the end of the clock period. The maximum frequency f_{max} corresponds to a minimum observation time t_{min} , and the nominal frequency f_{nom} to the nominal observation time t_{nom} .

Definition 2: Let φ be a gate delay fault, P a set of test patterns, and let $t \in [t_{min}, t_{nom}]$ be a point in time. Then t is called a *detecting observation time*, if φ is detected by capturing the test responses for P at time t . The set $I(\varphi)$ of all detecting observation times is called the *detection range of φ with respect to P* .

For each observation time in the detection range there is at least one circuit output and at least one test pattern, such that the fault free and faulty test responses are different. Figure 1 shows a simple example considering only a single output and a single test pattern.

Clearly the output waveforms differ, however, the fault effect is not visible at the nominal observation time t_{nom} . The detection range $I(\varphi)$ of φ is the union of the intervals in which the fault free and faulty waveform differ. Note that differences below the minimum observation time t_{min} are neglected. Figure 1 also shows that small glitches in the waveforms are not considered for the detection range due to pulse filtering in CMOS technology.

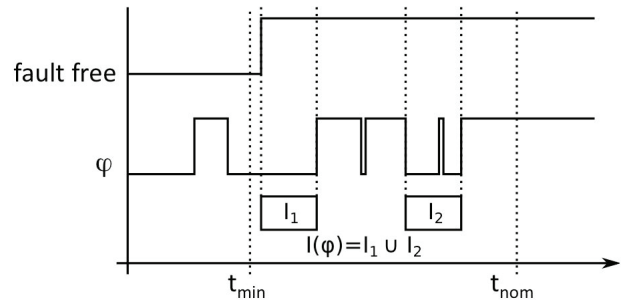


Figure 1. Detection range of a fault φ .

Based on the detection ranges for all HDFs, in [Hellebrand14] the selection of test frequencies has been formulated as the following optimization problem:

Optimum Frequency Selection: Given a set Φ of hidden delay faults and their detection ranges $I(\varphi)$ for all $\varphi \in \Phi$. Find a minimum set of observation times $T = \{t_0, \dots, t_{n-1}\}$, such that for each $\varphi \in \Phi$ the intersection $I(\varphi) \cap T$ is not empty. If there are two or more solutions with the same cardinality, select the one with larger observation times.

The problem *Optimum Frequency Selection* corresponds to a hitting set problem, which is an NP-complete problem [Karp72]. Therefore only a simple heuristic has been used in [Hellebrand14].

B. Accurate Timing Simulation

To limit the simulation effort for determining the detection ranges, in [Hellebrand14] only a symbolic path analysis was used. In this work, timing accurate simulation of small delay faults becomes feasible using the recently developed high-throughput simulation algorithm of [Schneider15]. It fully exploits data parallelism as well as structural parallelism inherent in patterns, gates, and faults by mapping the simulation task to a graphics processor (GPU).

The algorithm simulates signal waveforms and supports individual rising and falling pin-to-pin delays as well as glitch filtering at gates. It can correctly evaluate fault activation and propagation by glitches along reconvergent signals.

III. HYBRID FREQUENCY SELECTION

As already pointed out above, the proposed hybrid approach for frequency selection proceeds in several steps. The flow-chart of Figure 2 summarizes the procedure, the inputs of which are a set of test patterns P_{init} for transition delay faults, the nominal test frequency f_{nom} with observation time t_{nom} , the maximum possible frequency f_{max} with observation time t_{min} , and a parameter k specifying the number of equidistant frequencies.

In the preprocessing phase the transition faults detected by P_{init} are extracted and mapped to the initial fault set of potentially detectable small delay faults. Then a topological check sorts out all small delay faults for which either the longest topological path is too short to detect the fault at f_{max} or the shortest topological path is large enough to detect the fault at-

speed. In the first case that fault could only be detected with a frequency higher than f_{max} . In the second case the fault will always be detected by an at-speed test regardless of the actually sensitized path. The remaining faults are called *relevant* small delay faults.

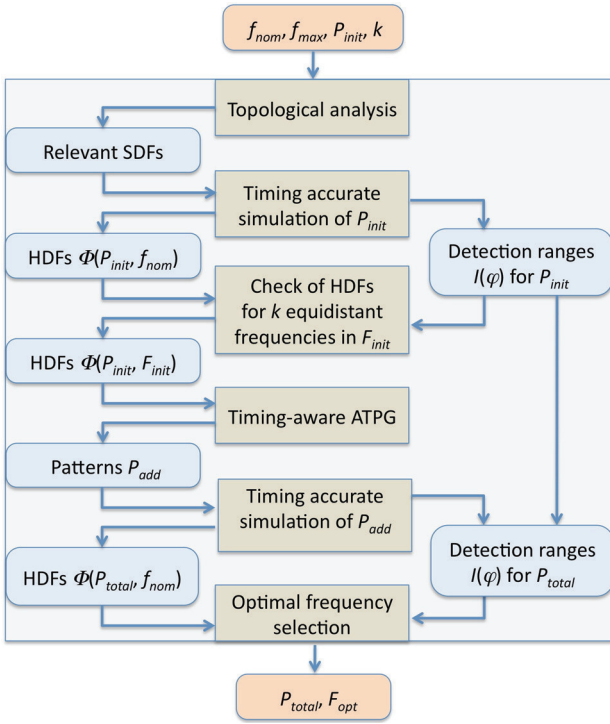


Figure 2. Workflow for frequency selection.

In the next step accurate timing simulation is performed for the relevant small delay faults to find the set of hidden delay faults $\Phi(P_{init}, f_{nom})$ as well as their detection ranges.

Then k equidistant frequencies are added to f_{nom} by defining k equidistant observation times t_0, \dots, t_{k-1} as follows:

$$t_0 = t_{min} = 0.3 \cdot t_{nom}, \text{ and}$$

$$t_i = t_{min} + i \cdot (t_{nom} - t_{min})/k, 0 < i < k.$$

This provides $T_{init} := \{t_0, \dots, t_{k-1}\}$ and the set of corresponding frequencies is denoted by F_{init} . The new observation times in T_{init} are checked against the detection ranges $I(\varphi)$ for all $\varphi \in \Phi(P_{init}, f_{nom})$. If the intersection $I(\varphi) \cap T_{init}$ is not empty, then φ can be deleted from $\Phi(P_{init}, f_{nom})$. As a result, the set of hard-to-detect hidden delays $\Phi(P_{init}, F_{init})$ is obtained.

For the faults in $\Phi(P_{init}, F_{init})$, additional test patterns are generated in the next step. Since $\Phi(P_{init}, F_{init})$ is usually small, more sophisticated ATPG methods can be used, e.g. timing-aware ATPG [Lin06], [Yilmaz10], [Zolotov10], [Eggersgluess11], [Sauer13]. This yields an additional set of test patterns P_{add} . Timing accurate simulation is performed again with the patterns from P_{add} . This determines the hidden delay faults $\Phi(P_{total}, f_{nom})$ with respect to $P_{total} := P_{init} \cup P_{add}$ and the nominal test frequency f_{nom} , as well as an update of the

detection ranges, such that for each fault $\varphi \in \Phi(P_{total}, f_{nom})$ the detection range $I(\varphi)$ is now available.

In the last step, the problem *Optimum Frequency Selection* is solved using the hypergraph algorithm described in [Shi10], a short summary of which can be found in section IV. The selection is based on the set of hidden delay faults $\Phi(P_{total}, f_{nom})$ and the updated detection ranges for P_{total} . The solution provides the final set of optimal frequencies F_{opt} guaranteeing maximum test efficiency. Please note that the preselected frequencies F_{init} are not necessarily contained in F_{opt} . Although the preselected frequencies in F_{init} may not be needed for the actual test, the experimental results will show that analyzing the low-cost scenario with F_{init} and P_{init} is an excellent strategy to identify the hard faults and direct timing-aware ATPG.

In all simulation and analysis steps, the detecting observation times are associated with the respective test patterns. Thus, for each frequency the actually required patterns from P_{total} can be selected without any extra effort.

IV. HYPERGRAPH-BASED OPTIMIZATION

This section briefly summarizes how the hypergraph algorithm in [Shi10] is applied to solve the problem *Optimum Frequency Selection*. A hypergraph $H = (V, E)$ consists of a set of vertices V and a set of edges $E \subset \mathcal{P}(V)$. The degree $deg(v)$ of a vertex $v \in V$ is the number of edges connected to v , while the degree of an edge $e \in E$ is its cardinality denoted by $rank(e)$. A discrete hitting set problem corresponds to the following hypergraph problem.

Minimum Hitting Set for Hypergraphs: Let $H = (V, E)$ be a hypergraph. Find a minimum hitting set $V_{hit} \subset V$, such that for each $e \in E$ the intersection $e \cap V_{hit}$ is not empty.

The algorithm described in [Shi10] performs depth first search in a binary tree to explore all possible candidates for V_{hit} . In each step it is decided whether a vertex is added to the solution or not. Vertices are considered in the order of decreasing degrees. Searching the complete tree guarantees the optimal solution $O(2^{|V|})$ time. To reduce the problem size as much as possible, the following reduction rules are applied before each decision in the search tree.

Vertex domination: For a vertex $v \in V$ let $h(v)$ denote the set of edges “hit” by v . If there are two vertices $v_1, v_2 \in V$, such that $h(v_1) \subset h(v_2)$, then v_1 can be replaced by v_2 in any solution, and thus can be removed from the hypergraph.

Edge domination: If there are two edges $e_1, e_2 \in E$ with $e_1 \subset e_2$, then each hit of e_1 is also a hit of e_2 , and e_2 can be deleted from the hypergraph.

Essential vertices: If there is an edge $e \in E$ containing only a single vertex $v \in V$, then v must be part of the solution.

Degree-2 neighborhood: For a vertex $v \in V$ define the degree-2 neighborhood as $B^2(v) := \{w \in V \mid v = w \text{ or there is an } e \in E \text{ with } e = \{v, w\}\}$. If there is a $v \in V$, such that the

number of edges connected to vertices in $B^2(v) \setminus \{v\}$ but not to v is smaller than $|B^2(v)| - 1$, then v is added to the solution.

While the first three rules are standard reduction rules for hitting set problems preserving the optimality of the solution, the fourth rule exploits the specific properties of degree-2 edges in hypergraphs. The overall runtime of the algorithm is $O(1.23801^{|V|})$, which makes the algorithm very attractive for larger problem instances [Shi10].

To map *Optimum Frequency Selection* to the *Minimum Hitting Set Problem for Hypergraphs*, the *atomic intervals* contained in the detection ranges are determined.

Definition 3: Let \mathcal{I} be a set of detection ranges. An interval I is considered as an *atomic interval* of \mathcal{I} , if it can be obtained as an intersection of intervals in the detection ranges and it is minimal with this property, i.e. if there is an interval J in the detection ranges with $I \cap J \subset I$, then $I \cap J = I$.

As illustrated in Figure 3 the atomic intervals are obtained by intersecting the time axis with the start and end points of all intervals in all detection ranges. The set of vertices V is then defined as the set of all atomic intervals.

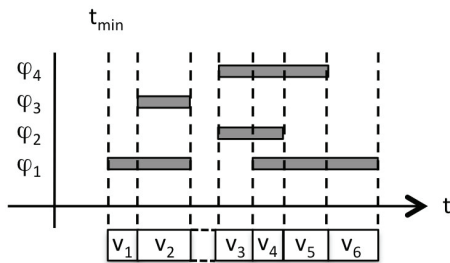


Figure 3: Mapping detection ranges to vertices.

The set of edges E is defined by creating an edge for each detection range and connecting it to all vertices hitting the detection range. Figure 4 shows the complete hypergraph for the example of Figure 3.

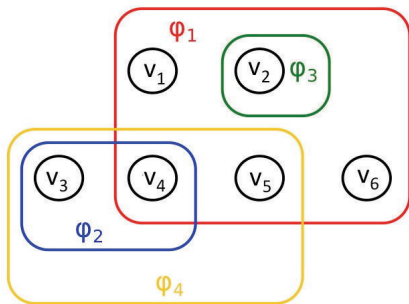


Figure 4: Hypergraph for the detection ranges of Figure 3.

Working with atomic intervals instead of just mapping the start and end points to vertices makes the problem formulation robust with respect to small process variations. No fixed observation times are associated with a solution, but rather small time windows for which the resulting FAST behavior is equivalent.

V. EXPERIMENTAL RESULTS

Experiments have been performed for a collection of ITC'99 [ITC99] and NXP benchmark circuits. Table I characterizes the analyzed circuits after synthesis for a 90 nm technology library. The columns show the number of gates, the number of primary and pseudo-primary inputs, as well as the number of primary and pseudo-primary outputs.

TABLE I. ANALYZED CIRCUITS

Circuit	Gates	PIs+PPIs	POs+PPOs
b14 1	12438	260	214
b15 1	6533	572	418
b17 1	21858	1827	1348
b18 1	75618	4116	3085
b20 1	25547	533	450
b21 1	25561	534	450
b22 1	38568	786	664
p45k	22414	3739	2550
p78k	46504	3148	3484
p81k	78665	4029	3952
p89k	56662	4627	4557
p100k	53836	5902	5829
p141k	105347	11290	10502

The initial set of test patterns P_{init} has been generated by a commercial tool targeting transition faults (TF), and the additional set P_{add} has been obtained by performing timing-aware ATPG with the same tool. Table II shows the number initial number of small delay defects in column 2. As explained in section III, these faults correspond to the small delay faults which are potentially detectable by P_{init} . The number of relevant small delay faults after topological analysis is reported in column 3. Finally column 4 lists the number of hidden delay faults with respect to P_{init} and the nominal test frequency f_{nom} .

TABLE II. SMALL AND HIDDEN DELAYS AT NOMINAL FREQUENCY

Circuit	# SDF	# Relevant SDFs	# HDFs $\Phi(P_{init}, f_{nom})$
b14 1	25126	20956	18972
b15 1	31504	15201	6817
b17 1	97878	62464	50777
b18 1	255960	147859	120470
b20 1	59155	50058	49855
b21 1	59761	50170	46631
b22 1	93262	81291	75642
p45k	127295	74851	66742
p78k	268989	232626	203575
p81k	434642	383678	372728
p89k	314225	216031	193019
p100k	301279	169612	149800
p141k	575885	338336	317576

For almost all circuits the timing aware patterns in P_{add} are not able to detect any additional small delays at nominal frequency. Only for circuit p78k one additional fault is detected at speed.

Table III shows the results of the hybrid frequency selection described in Section III. For all circuits, $k = 6$ equidistant frequencies were preselected.

TABLE III. RESULTS OF OPTIMAL FREQUENCY SELECTION

Circuit	P_{init}			P_{total}		
	# Pattern pairs	HDF coverage with F_{init}	# Frequencies for 100% test efficiency	# Pattern pairs	HDF coverage with F_{init}	# Frequencies for 100% test efficiency
b14 1	655	94.61%	23	885	96.61%	19
b15 1	302	85.14%	17	1102	94.28%	12
b17 1	492	93.59%	32	1438	95.82%	24
b18 1	1002	93.46%	30	2726	95.55%	26
b20 1	943	96.57%	28	1513	98.43%	20
b21 1	928	96.31%	29	1587	98.23%	22
b22 1	1109	96.59%	35	2129	98.61%	25
p45k	2756	97.73%	12	7888	98.08%	12
p78k	51	99.49%	25	252	99.92%	14
p81k	311	98.68%	34	4892	99.17%	31
p89k	797	95.39%	36	3695	97.26%	31
p100k	2633	96.37%	34	6736	97.43%	24
p141k	812	97.25%	54	7305	98.87%	34

Columns 2 to 4 show the results achievable with the initial test set P_{init} . The number of pattern pairs is given in the second column. The percentages in the third column show that using the preselected frequencies in F_{init} already a large part of the initially hidden delay faults in $\Phi(P_{init}, f_{nom})$ can be detected, but complete coverage of all relevant small delay faults is not possible. For comparison, the fourth column shows the optimal number of frequencies required to obtain maximum test efficiency, when the algorithm only uses the detection ranges for P_{init} . Columns 5 to 7 present the same analysis for the combination of transition delay and timing-aware patterns in P_{total} . The hidden delay faults targeted in this step are the faults in $\Phi(P_{total}, f_{nom})$. The results show that working with P_{total} considerably improves the results in both cases. Overall, Table III shows that maximum test efficiency, and thus complete coverage of all relevant small delay faults, is possible with at most 34 frequencies when the options of a commercial ATPG tool are properly exploited.

The required number of frequencies can be further reduced, if a small reduction of test efficiency is accepted. To illustrate this, Figure 5 shows the test efficiency as a function of the number of frequencies for circuit p141k. The solid line corresponds to the results of frequency selection working with the initial test P_{init} only, and the dotted line characterizes the results with P_{total} . As the remaining circuits exhibit similar behavior, the respective results are not displayed for simplicity. The curves in Figure 5 show that a relatively high coverage of relevant small delay faults can already be reached with very few frequencies (usually less than 10). Moreover, relying on a combination of transition fault and timing-aware patterns provides a much faster increase in test efficiency as indicated by the steeper curve.

As already discussed in Section III, the preselected frequencies F_{init} may not be part of the solution. As shown in the figure, the circuit contains a few extremely hard faults. Consequently, the optimal solution contains many frequencies that detect only a single fault. Although it is very difficult to reach

maximum test efficiency, the proposed approach can achieve this goal with a minimum number of frequencies.

Due to the high reduction achieved by the timing-aware patterns the number of frequencies is still within an acceptable range. Verified by timing-accurate fault simulation, it provides the maximum efficiency for a test with frequencies technically limited by f_{max} . The computing time for the hybrid frequency selection is dominated by the timing-accurate fault simulation. For the largest circuit p141k, the simulation time is in the range of several hours, while the hypergraph algorithm for frequency selection only needs a few seconds.

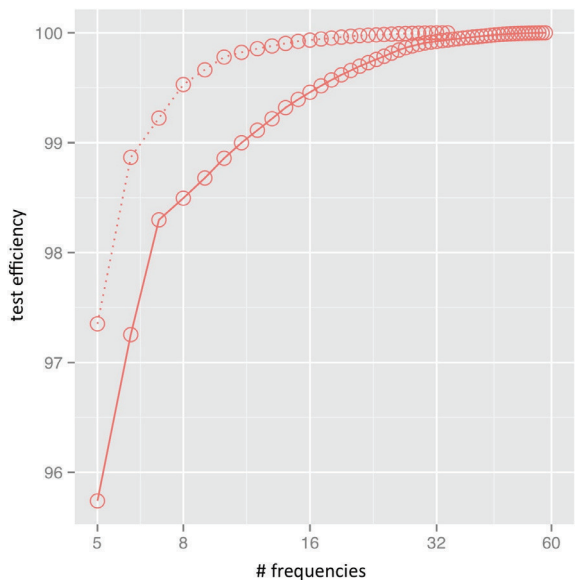


Figure 5. Test efficiency for circuit p141k as a function of the number of frequencies used with P_{init} (solid lines) and with P_{total} (dashed lines).

VI. CONCLUSIONS

Implementing faster-than-at-speed with preselected equidistant frequencies allows a simple setup, but it cannot guarantee complete coverage of hidden delay faults.

Nevertheless, an analysis of this scenario with a basic test set helps to identify the hard faults and guide timing-aware ATPG. The presented approach combines transition delay patterns with timing-aware patterns for the hard faults to derive an optimal selection of frequencies. The solution guarantees maximum test efficiency with a minimum number of frequencies not exceeding f_{max} . The solution is verified by exact timing-aware fault simulation. Furthermore, it is robust against small delay variations, as each selected frequency corresponds to a small time window for which the resulting FAST behavior is equivalent.

ACKNOWLEDGEMENT

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