Variation-Aware Deterministic ATPG

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Preprint

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Variation-Aware Deterministic ATPG

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Abstract—In technologies affected by variability, the detection status of a small-delay fault may vary among manufactured circuit instances. The same fault may be detected, missed or provably undetectable in different circuit instances. We introduce the first complete flow to accurately evaluate and systematically maximize the test quality under variability. As the number of possible circuit instances is infinite, we employ statistical analysis to obtain a test set that achieves a fault-efficiency target with an user-defined confidence level. The algorithm combines a classical path-oriented test-generation procedure with a novel waveform-accurate engine that can formally prove that a small-delay fault is not detectable and does not count towards fault efficiency. Extensive simulation results demonstrate the performance of the generated test sets for industrial circuits affected by uncorrelated and correlated variations.

Keywords—Variation-aware test, fault efficiency, ATPG

I. INTRODUCTION

Recent semiconductor manufacturing technology nodes are heavily affected by massive parameter variations which create severe challenges for design and test of state-of-the-art circuits [1, 2]. Manufacturing defects interact with the effects of variations in complex and often unpredictable ways. This holds in particular for small-delay faults, which are defined as fixed amounts of extra delay at a given gate. Traditional fault-coverage metrics and test-generation methods are insufficient for circuit populations affected by variations. They ignore the fact that a given test set could detect a fault in some manufactured instances of the circuit but miss the same fault in other instances. The fault may also be provably undetectable in some of the instances, and such faults should not count towards fault efficiency. However, the parameters affected by variability, i.e., delays, are continuous and the number of possible circuit instances is infinite.

A further substantial difficulty in variation-aware testing is the reliance of traditional test methods on the concept of path sensitization [3, 4]. It is assumed that, in order to detect a small-delay fault \( f \) on a given gate, it is sufficient to find a test pair that sensitizes the longest path that goes through that gate. However, even in absence of variations, such procedures are not suited to identify undetectable faults. They enforce certain sensitization conditions, including robust, non-robust and functional sensitization. If no robustly sensitizable path of sufficient length (that is, cumulative delay) exists through the fault location, the fault is not proven undetectable, as detection through non-robustly or functionally sensitized path could be possible. On the other hand, non-robust or functional sensitization is prone to invalidation, and faults for which such a path has been found may actually not be detected [5]. This situation is even worse under variations where the same path may have a length that is sufficient for detection in one instance but not sufficient in another.

In this paper, we present a statistical metric that generalizes the concept of fault efficiency (FE) to circuits under variations. We assume that variations are described by a known probability distribution, which may be correlated or uncorrelated. The metric consists of three parts: fault efficiency bound \( F E_{\text{min}} \), probability \( c \) and confidence \( \gamma \). An individual circuit instance \( i \) has fixed delays, and the fault efficiency (FE) of a test (pair) set \( T \) with respect to an instance \( i \) is the number of faults detected by \( T \) divided by the number of detectable faults in \( i \). Under variations, there are infinitely many instances \( i \), and the same test set \( T \) may have different \( FE \) on different instances. \( T \) achieves fault efficiency \( F E_{\text{min}} \) with probability \( c \) if the share of instances on which the fault efficiency of \( T \) is equal to or greater than \( F E_{\text{min}} \) is at least \( c \). In other words, if a large number \( N \) of random circuit instances is drawn according to the known probability distribution, at least \( c \cdot N \) of them will have \( F E \geq F E_{\text{min}} \) and at most \( (1-c) \cdot N \) may have \( F E < F E_{\text{min}} \).

We introduce an automatic test generation algorithm that produces a test set that achieves \( F E_{\text{min}} \) with probability \( c \). This property of the test set holds with confidence level \( \gamma \). The probability distribution and the parameters \( F E_{\text{min}}, c \) and \( \gamma \) are inputs of the algorithm. Larger values of these parameters result in a larger test set. In contrast to previous variation-aware test generation approaches [6–12], the proposed algorithm relies on accurate fault efficiencies of the generated test sets. For this reason, the algorithm employs a very recently introduced SAT-based test-generation engine WaveSAT [5] that works with waveform precision and does not rely on path sensitization. WaveSAT is able to accurately classify a given fault, that is, to generate a test pair that detects it or to prove that the fault is undetectable and should be removed from fault efficiency calculation.

We applied our algorithm to mid-size industrial circuits and were able to generate test sets for large values (\( \geq 0.98 \)) of \( F E_{\text{min}}, c \) and \( \gamma \). The approach is validated on uncorrelated and correlated probability distributions. The scalability is achieved by complementing WaveSAT by a fast timing-aware path-
sensitization procedure PHAETON [13, 14] and an efficient parallel delay fault simulator fsim running on general-purpose graphics processing units (GPGPUs) [15].

The remainder of the paper is organized as follows. Section II provides background on variation-aware test and the metrics used in this paper. It also introduces the statistical model of fault detection with a guaranteed confidence level. Section III starts with a brief review of procedures which generate test pairs for faults in circuit instances with fixed delays. The discussion of these procedures and their properties is essential as they are the basis of the adaptive confidence-guided algorithm, which is presented in the remainder of Section III. Experimental results are reported in Section IV. Section V concludes the paper.

II. VARIATION-AWARE TEST

A. Circuit model under variations

We assume that variability affects the delays of all gates of a circuit while leaving its topology unchanged. Therefore, gate delays are random variables described by a probability distribution. While uncorrelated variations have been predicted to be dominant in the nanoscale technologies [16–18], our approach is based on Monte-Carlo experiments and therefore works independent of the distribution. We will report experimental results for both uncorrelated and uncorrelated variations. In this paper, we assume circuits composed of primitive gates and a simplified timing model: each gate $g_i$ has an input-to-output delay $p_i$. Each $p_j$ is a random variable, and a circuit $C$ with $n$ gates is completely described by a parameter configuration $p = (p_1, \ldots, p_n)$. This model can be easily extended by incorporating different rising and falling delays, pin-to-pin delays and pattern-dependent delays, resulting in more random variables per circuit. It is also possible to include travel times on wires and pulse filtering.

A circuit $t = C[p]$ where all gate delays have fixed values $(p_1, \ldots, p_n)$ is called a circuit instance or simply an instance. The nominal instance $t_0$ has all delays set to the expected values of their distributions. When circuits are manufactured, each produced circuit is described by an instance. Manufacturing $N$ circuits corresponds to a Monte-Carlo experiment where the parameters $(p_1, \ldots, p_n)$ of each instance are drawn according to the distribution. It is possible to simulate this process by drawing sets of random parameters without actually manufacturing the circuit. This Monte Carlo simulation yields a set of instances called population. Properties that are valid for the simulated population of sufficient size hold for different populations, including the actual manufactured circuits, with some probability called confidence level.

B. Fault detection under variations

We consider small-delay faults (SDFs) that are defined at logic gates in the circuit. An SDF $(g, s)$ results in a slow-down of gate $g$ by $s$ time units. An SDF is detected by a test pair $(v_1, v_2)$ if the circuit affected by this SDF has an incorrect value on at least one output at the observation time $t_{obs}$. We define $t_{obs}$ as the time when the circuit’s outputs are read out. $t_{obs}$ typically equals the clock cycle duration, and a (fault-free) circuit instance in which all possible transitions are finished before $t_{obs}$ is called timing-correct. We assume that the value of $t_{obs}$ is not affected by variations and is hence equal for all circuit instances in the population. Under normal circumstances, the designer will set $t_{obs}$ such that the majority of (fault-free) circuit instances in a population are timing-correct and only a few instances have delays $(p_1, \ldots, p_n)$ that are so large that $t_{obs}$ is exceeded. Such instances contribute to the parametric yield loss and are not considered here.

Detection of an SDF in two individual instances of the same circuit, $i_1$ and $i_2$, is illustrated in the left and the right part of Figure 1, respectively. The SDF of size $\varepsilon = 3.5$ would be detected in instance $i_1$ (transition on the output at time 10.5, after $t_{obs} = 8$) and not detected in instance $i_2$ (output transition at time 7.5, before $t_{obs}$). However, this fault is detectable in instance $i_2$ through path B-g1-g2-g4, sensitized by a different test pair $AB = 11/10$ and inducing the output transition at time 8.5.

A fault is undetectable if there is no path of sufficient length ($\geq t_{obs} - s$) through its location. We refer to this case by the term structural undetectability. In our example, the SDF on g1 with size $\varepsilon = 2$ is detected in instance $i_1$ but structurally undetectable in instance $i_2$. If a sufficiently long path does exist, it may or may not be possible to find a test pair that sensitizes it such as to induce the incorrect value at time $t_{obs}$.

In summary, a given test set $T$ partitions the set $F$ of all considered SDFs in circuit instance $i$ into three parts: $F = F_{det}(i, T) \cup F_{ind}(i) \cup F_{miss}(i, T)$, where $F_{det}(i, T)$, $F_{ind}(i)$ and $F_{miss}(i)$ are the sets of faults detected by $T$ in instance $i$, faults that are provably undetectable in instance $i$, and faults that are detectable in $i$ but have been missed by $T$, respectively. Note that $F_{ind}(i)$ depends on the instance (the same fault could be undetectable in some instances and detectable in others) but not on test set $T$. The fault efficiency of a test set $T$ with respect to a fault set $F$ in an instance $i$ is

$$FE(F, T, i) = \frac{|F_{det}(i, T)|}{|F \setminus F_{ind}(i)|}.$$  \hspace{1cm} (1)

It is important to point out the significance of the set $F_{ind}(i)$ of undetectable faults. When stuck-at faults are considered, most circuits have no or very few undetectable faults. In case of small-delay faults considered here, the detection depends on the relationship between the slack of the sensitized path (the difference between $t_{obs}$ and its length) and the size $s$ of the SDF. If many SDFs have a size that is close to the slack of a sensitizable path, they may be detectable in some circuit instances but undetectable in others. Fault coverage metrics employed in previous work [19] that did not incorporate
Therefore, the confidence for $F$ and $T$ establishes the formal relationship between instances in a row which raises the confidence. We will now consider the test set $F_E$ and an excessively high fault efficiency $F_E$ random instance is evaluated and if its fault efficiency exceeds $k$ and the probability of achieving $F_E$ is less than or equal to $F_{E_{\text{min}}}$ with a probability of $\tilde{c}$. Now, the confidence level $\gamma$ captures the probability that this positive result of the Monte-Carlo experiment implies $\tilde{c}$ is less than the desired probability $c$. Hence, the result of Monte-Carlo experiment was positive and missed to the belief that the probability is no less than $c$ while in reality it was $\tilde{c} < c$.

The probability for this opposite event is $(1 - \gamma)$. Therefore, the probability of the positive result of the Monte-Carlo experiment, or $\tilde{c}$, must be less than $(1 - \gamma)$ for all $\tilde{c} < c$. From $\tilde{c} \leq 1 - \gamma$ for all $\tilde{c} < c$, it follows $\tilde{c} \leq 1 - \gamma$. This implies that in order to obtain a desired confidence level $\gamma$, the following number $k$ of instances must be considered:

$$k \geq \left\lceil \frac{\ln(1 - \gamma)}{\ln(c)} \right\rceil.$$  

Eq. 3 delivers $k$ with the following property. If a test set $T$ is applied to $k$ randomly generated instances and exceeds fault efficiency $F_{E_{\text{min}}}$ for all of them, then the probability that an arbitrary randomly generated circuit instance will exceed fault efficiency $F_{E_{\text{min}}}$ is $c$ with confidence $\gamma$. This property will be utilized in the adaptive test generation procedure in Section III.

### III. CONFIDENCE-GUIDED TEST GENERATION

The confidence-guided test generation procedure aims at producing a test set $T$ that achieves a certain desired fault efficiency $F_{E_{\text{min}}}$ on any arbitrary instance with probability $c$ and confidence $\gamma$. As explained in Section II-C, a test set $T$ fulfills this condition if it exceeds $F_{E_{\text{min}}}$ for $k$ randomly generated circuit instances, where $k$ is calculated using Eq. 3.

The pseudo-code of the procedure is found in Algorithm 1. Before the algorithm is explained, key sub-routines called by the method and their relevant properties are outlined.

- **PHAETON** is a SAT-based path-oriented small-delay test pattern generator [13, 14]. Given a set of faults $F$ and a circuit instance $i$, it searches, for each fault $f \in F$, for the longest path through the fault location that can be sensitized in $i$ and calculates the test pair that does the sensitization. In this work, PHAETON uses robust path sensitization.
sensitization that is not prone to invalidations but may miss detectable faults.

- **WaveSAT** is a small-delay ATPG engine that generates timed sequences of rising and falling transitions (waveforms) on the circuit lines [5] that lead to the detection of the fault. Since WaveSAT does not necessarily sensitize the longest possible path, its generated test pair do not tend to detect many faults. However, WaveSAT allows accurate classification: if no test pair is found, it is guaranteed that none exists, i.e., the fault is undetectable under the given timing assumptions. WaveSAT is used for two purposes: close the gaps in fault coverage by pinpointedly generating test pairs for faults missed by PHAETON test pair sets, and prove that a fault is undetectable in a specific circuit instance and can be excluded from fault-efficiency calculation.

- **fsim** is a delay fault simulator that runs in parallel on general-purpose graphic processing units (GPGPUs) [15]. The high degree of parallelization is beneficial when grading a large number of circuit instances that have the same structure but different delays.

To construct $T$ with the desired property, the nominal instance $i_0$ and a number of further instances $i_1, i_2, \ldots$, called the training set, are considered (the number of instances in the training set is not known ahead of time, as new instances are added to the training set until the test set reaches the required quality). The initial $T$ is generated to obtain 100% fault efficiency on the nominal instance $i_0$ in Lines 1 through 4 of Algorithm 1. PHAETON is used to quickly generate a good test set and WaveSAT to cover the missed faults identified by fsim. In Line 5, the number $k$ of circuit instances that need to be considered to obtain the fault-efficiency estimate with the desired confidence $\gamma$ is calculated according to Eq. 3. Then, Lines 7 through 16 are repeated until the test set $T$ fulfills the $FE$ target, that is, exceeds $FE_{\text{min}}$ for $k$ consecutive random instances $i$. This is implemented as follows.

The random instance $i$ is generated in Line 8, and the faults $F_{\text{det}}$ detected by $T$ are determined by fault simulation in Line 9. The set of undetectable faults $F_{\text{nd}}$ is obtained by running WaveSAT and collecting all faults shown to be undetectable. In addition, WaveSAT generates top-up test pairs for faults not detected by the initial $T$; these pairs are collected in set $T_{\text{tu}}$. If at least one of $k$ instances does not reach fault efficiency of $FE_{\text{min}}$, the top-up pairs are added to $T$ and another $k$ instances are considered (this is achieved by setting the loop variable $j$ to 0). The iterations stop when $T$ exceeds $FE_{\text{min}}$ for $k$ instances in a row. This means that $T$ is of sufficient quality and fulfills the specification; therefore, this $T$ is returned in Line 18.

### IV. Experimental Results

#### A. Explicit test generation for random circuit instances

To evaluate the need for considering variations during test generation, we performed the following experiment for combinational cores of industrial circuits provided by NXP. For each circuit, we generated one nominal instance $i_0$ with all delays set to their nominal values, and 1000 instances $i_1, \ldots, i_{1000}$ with delays described by independent random variables according to a Gaussian distribution with standard deviation of 20%. We considered small-delay faults at 100 randomly chosen but fixed fault locations (gates) with nine different sizes equiprobably distributed across the clock cycle, i.e., 10% of $t_{\text{obs}}$, 20% of $t_{\text{obs}}$, through 90% of $t_{\text{obs}}$. A substantial portion of these faults are provably undetectable, as no sensitizable path of sufficient length exists through their location. We generated a number of test sets $T_N$ with complete coverage of detectable faults (fault efficiency of 100%) on the instances $i_0$ through $i_N$. This has been done by running PHAETON on $i_0$, simulating the generated test set on instances $i_0, \ldots, i_N$, and using WaveSAT to either detect all undetected faults or classify them as provably undetectable. For example, test set $T_{10}$ detects all detectable faults in the nominal instance $i_0$ and ten further instances $i_1$ through $i_{10}$.

The quality of test sets $T_N$ is reported in Columns 6–15 of Table I (the numbers for 5-detect and 10-detect timing-aware transition fault test sets generated by a commercial tool by sensitizing the longest path through a fault location are given in Columns 4 and 5 for reference). Column 3 contains the number of detectable faults aggregated over all 1001 instances. For each test set, the size of the test set |$T$|, the number |$F$| of detected faults in all instances and the fault efficiency $FE$, obtained by dividing this number by the value in Column 3, are quoted. It can be seen that the fault efficiency of variation-
The size only moderately with the size of the training set. For likelihood that the generated test set pattern generation time $c$ of instances with $\gamma$ instances ($\gamma$ the statistical test of Eq. 3; the size $T$ random circuit instances considered before test combination. $k$ the respective value of $\gamma$ experiment), the fault-efficiency target $F E$ algorithm takes the circuit, the fault set (same as in the first $\gamma$ is reported in Table III. Recall that the $F E$ $c$ level $F E$ of the training set, that is, the number of $F E$ processed cards with 1.6GB RAM.

It can be seen that the obtained test sets are of extremely high quality. The average $F E$ substantially exceeds the target $F E_{\min}$ in all cases. The percentage $\tilde{c}$ of individual instances for which the test sets exceed $F E_{\min}$ is always much larger than the target value $c$, and in most cases even reaches 100%. The runtimes associated with the confidence-driven test generation are moderate and do not exceed a few hours, even for large circuits under high confidence and probability targets. Recall that the test sets are evaluated on random circuit instances unrelated to the ones for which they have been generated. Interestingly, while the number of considered instances $I_{\gamma}$ appears to scale with $k$, the differences between the test set sizes and fault efficiencies reached for a fixed circuit are rather small.

We also applied the test sets (that were obtained assuming uncorrelated variations) to a population that consists of 1025 correlated instances. The correlated instances were drawn from a two-dimensional parameter space that describes gate delay distributions with multiple gradients and different orientations in order to model spatial correlations. This parameter space has the same mean and variance over all instances as compared to the random cases.

The results can be found in Table IV. Columns $F E$ quote the average fault efficiency of the generated test set among all the correlated instances, and columns $\tilde{c}$ contain the percentage of instances with $F E$ exceeding $F E_{\min}$. It can be seen that test sets generated assuming no correlations are highly effective even in presence of (unexpected) correlations. One explanation for this is the fact that the set of possible combinations of delay value in the uncorrelated case is a strict superset of any corresponding set for the correlated case. In other words, any delay combination that can occur in presence of correlations can also occur in absence of correlations, and there is some chance that a test pair for this combination is included in test set $T$.

All experiments have been conducted on a host system equipped with Intel Xeon processors clocked at 2.8GHz, 256GB RAM and NVIDIA GeForce GTX 480 graphics processing cards with 1.6GB RAM.

<table>
<thead>
<tr>
<th>Circuit Gates Detectable</th>
<th>Timing-aware for $i_{10}$</th>
<th>Variation-aware test sets $T_N$ generated for instances $i_0, \ldots, i_N$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p4k$ 25679 210290</td>
<td>$</td>
<td>T</td>
</tr>
<tr>
<td>$p78k$ 70475 434292</td>
<td>$\tilde{T}$</td>
<td>$110$ $215$ $317$ $363$ $386$ $421$ $449$ $489$ $531$ $581$ $602$ $655$ $686$</td>
</tr>
<tr>
<td>$p89k$ 58638 155318</td>
<td>$\tilde{T}$</td>
<td>$41$ $75$ $605$ $672$ $734$ $849$ $993$ $1175$ $1401$ $1675$ $1774$ $1967$ $2096$</td>
</tr>
<tr>
<td>$p100k$ 61066 201883</td>
<td>$\tilde{T}$</td>
<td>$95$ $192$ $284$ $309$ $322$ $355$ $381$ $416$ $462$ $515$ $538$ $575$ $594$</td>
</tr>
</tbody>
</table>

**Table I**

Test set size $|T|$, numbers of detected faults $|F|$ and fault efficiency $F E$ [%] over 1001 circuit instances (9 fault sizes).

**Table II**

Value of $k$ depending on target probability $c$ and confidence $\gamma$.

<table>
<thead>
<tr>
<th>$\gamma$</th>
<th>$c = 0.98$</th>
<th>$k = 149$</th>
<th>$c = 0.985$</th>
<th>$k = 199$</th>
<th>$c = 0.99$</th>
<th>$k = 228$</th>
<th>$c = 0.99$</th>
<th>$k = 259$</th>
<th>$c = 0.99$</th>
<th>$k = 305$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tilde{c}$</td>
<td>0.95</td>
<td>0.98</td>
<td>0.99</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TABLE III
NUMBER OF CONSIDERED INSTANCES | I_c | TEST SET SIZE | T(I_c) | PATTERN GENERATION TIME T_p, SIMULATION TIME T_s, FAULT EFFICIENCY FE AND ACTUAL PERCENTAGE OF SUFICIENTLY COVERED INSTANCES $\tilde{c}$ FOR FAULT-EFFICIENCY TARGET \( FE_{\text{target}} \), TARGET PROBABILITY \( \tilde{c} \) AND CONFIDENCE $\gamma$.

| Circuit | $|I_c|$ | $|T(I_c)|$ | $T_p$ [s] | $T_s$ [s] | $FE$ [%] | $\tilde{c}$ | $|I_c|$ | $|T(I_c)|$ | $T_p$ [s] | $T_s$ [s] | $FE$ [%] | $\tilde{c}$ | $|I_c|$ | $|T(I_c)|$ | $T_p$ [s] | $T_s$ [s] | $FE$ [%] | $\tilde{c}$ |
|---------|-----|--------|--------|--------|--------|--------|-----|--------|--------|--------|--------|--------|-----|--------|--------|--------|--------|--------|--------|
| p45k    | 46  | 2534   | 108    | 94.7   | 99.7   | 99.7   | 54  | 107    | 94.6   | 98.9   | 99.6   | 99.6   | 54  | 107    | 94.6   | 98.9   | 99.6   | 99.6   | 54  | 107    | 94.6   | 98.9   |
| p78k    | 92  | 3490   | 213    | 94.3   | 99.3   | 99.3   | 188 | 210    | 94.1   | 98.6   | 99.5   | 99.5   | 188 | 210    | 94.1   | 98.6   | 99.5   | 99.5   | 188 | 210    | 94.1   | 98.6   |
| p89k    | 131 | 4930   | 283    | 94.0   | 99.0   | 99.0   | 263 | 283    | 93.9   | 98.4   | 99.3   | 99.3   | 263 | 283    | 93.9   | 98.4   | 99.3   | 99.3   | 263 | 283    | 93.9   | 98.4   |
| p100k   | 162 | 6371   | 351    | 93.8   | 99.3   | 99.3   | 381 | 351    | 93.7   | 98.2   | 99.2   | 99.2   | 381 | 351    | 93.7   | 98.2   | 99.2   | 99.2   | 381 | 351    | 93.7   | 98.2   |

TABLE IV
TEST SET VALIDATION ON 1025 CORRELATED INSTANCES.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>$FE$ [%]</th>
<th>$\tilde{c}$</th>
<th>$FE$ [%]</th>
<th>$\tilde{c}$</th>
<th>$FE$ [%]</th>
<th>$\tilde{c}$</th>
<th>$FE$ [%]</th>
<th>$\tilde{c}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>p45k</td>
<td>99.276</td>
<td>91.4</td>
<td>99.276</td>
<td>91.4</td>
<td>99.276</td>
<td>91.4</td>
<td>99.276</td>
<td>91.4</td>
</tr>
<tr>
<td>p89k</td>
<td>99.308</td>
<td>85.2</td>
<td>99.308</td>
<td>85.2</td>
<td>99.308</td>
<td>85.2</td>
<td>99.308</td>
<td>85.2</td>
</tr>
<tr>
<td>p100k</td>
<td>99.342</td>
<td>91.3</td>
<td>99.342</td>
<td>91.3</td>
<td>99.342</td>
<td>91.3</td>
<td>99.342</td>
<td>91.3</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

We presented the first test generation method that produces test sets with proven statistical performance under variations. Its core procedure iteratively enriches the test set by explicitly considering random circuit instances, guided by an estimated confidence level. The method employs the latest SAT-based timing-aware test generation engines which can provide complete testability characterization of all faults in a circuit instance, thus extending the concept of fault efficiency to variation-aware testing for the first time. The obtained test sets guarantee a minimum fault efficiency on all instances with user-defined probability and confidence bounds. The method is applicable to industrial circuits.

VI. ACKNOWLEDGMENT

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