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Diagnosis of Multiple Faults with Highly Compacted Test Responses

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***Abstract*—Defects cluster, and the probability of a multiple fault is significantly higher than just the product of the single fault probabilities. While this observation is beneficial for high yield, it complicates fault diagnosis. Multiple faults will occur especially often during process learning, yield ramp-up and field return analysis.**

In this paper, a logic diagnosis algorithm is presented which is robust against multiple faults and which is able to diagnose multiple faults with high accuracy even on compressed test responses as they are produced in embedded test and built-in self-test. The developed solution takes advantage of the linear properties of a MISR compactor to identify a set of faults likely to produce the observed faulty signatures. Experimental results show an improvement in accuracy of up to 22 % over traditional logic diagnosis solutions suitable for comparable compaction ratios.

***Index Terms*—Multiple Faults, Diagnosis, Response Compaction**

I. Introduction

Defects cluster, and the probability of multiple defects on a single die is significantly higher than the square product of the single defect probability. This early observation in semiconductor manufacturing led to more sophisticated yield models than the Poisson model [1], [2], and it is even more valid today when systematic and parametric faults may affect regions of a circuit.

Multiple faults are specially relevant in two phases of the lifecycle: In the yield learning phase when new designs and manufacturing processes are introduced, defect density is still high and multiple faults cannot be neglected. During the system's lifecycle field returns may have to be analyzed, which can be subject to many effects like external stress, ageing and of course design flaws. Again, these mechanisms affect the entire die and multiple faults have to be expected.

Fortunately, during test and test generation multiple faults are not such a big challenge, as it is known that test pattern sets generated under the single fault assumption are also very effective for multiple faults [3]. The situation is completely different for logic diagnosis. For most diagnostic algorithms the presence of just a second fault creates a distraction which prevents the exact location of both of them. While changing a single fault model, let us say transition instead of stuck-at faults, requires mostly incremental changes of the diagnostic algorithms, the consideration of multiple faults enforces major modifications.

The situation is aggravated if during diagnosis the chip infrastructure for test compression and response compaction is used. During production test this infrastructure is mandatory for economic reasons, and it is expensive to switch it off for diagnostic purposes. While state-of-the-art diagnostic solutions support the compaction of scan tests [4], [5], other applications like, for example, system test [6], [7] and field return analysis [8], [9] make use of built-in self-test (BIST) infrastructure to gather failure response data. For such applications with higher compaction requirements, the diagnosis of multiple faults is still an open challenge.

The goal of the paper at hand is to present the first technique which can use compaction schemes based on linear signature registers in order to diagnose multiple faults with very high efficiency. This diagnostic technique is specially useful to support non-destructive diagnostic procedures after system assembly. The basic idea of the new algorithm is the introduction of a *disturbance function*. If two faults are in different regions of a circuit, they do not affect each other and they can be analyzed by standard diagnostic techniques using superposition. However, if the output cones of these faults overlap, the fault effect is not anymore the combination of the single fault outputs, and the disturbance function describes this difference.

The rest of the paper is organized as follows. In the next section, previous work is discussed. In Section III, the basic concept of the disturbance function is explained, and in Section IV the novel signature-based diagnostic procedure is detailed. Section V presents experimental results showing the significant increase in resolution.

II. Previous Work

The diagnosis of multiple faults has already been studied mainly in the context of manufacturing test [10], [11], [12], [13], [14], [15]. The paper at hand follows the approach of [15] which introduced the conditional stuck-at faults or conditional line flips. A conditional fault is described by a signal x and a very general conditional $cond(\vec{y})$, and denotes that line x is inverted if the condition evaluates to true: $f_x = cond(\vec{y}) \oplus x$. $\vec{y}$ may describe Boolean values of different lines, a timing behavior or even a random event in case of intermittent faults.

Embedded test and BIST infrastructure may support diagnosis, since more patterns can be applied in shorter time without the need of expensive external ATE resources [16]. However, the compacted response information in the signature registers pose extra challenges for diagnosis, and often such diagnostic methods for BIST may require several test sessions to identify faulty test patterns. However, due to bandwidth and tester memory limitations, only a few faulty test patterns are usually considered for logic diagnosis. Test sessions may target specific scan elements [17], [18], [19], [20] or work on different patterns [21], [22]. In these approaches, the values captured by the scan elements need to be obtained directly from the

tester or computed from the observed compacted responses. The latter approach is often called *indirect diagnosis*.

Conversely, *direct diagnosis* employs diagnostic algorithms specially devised for the analysis of compacted test signatures in order to infer a faulty chip location. Such a direct approach has been proposed in [6], where the authors achieve high diagnostic resolution from the failure responses produced by a MISR. More recently, the works in [23], [8] achieve larger compaction ratios to efficiently store test responses on-chip and do not require multiple test sessions. These direct diagnosis approaches for BIST extend the *single location at a time* (SLAT) paradigm [24]. A faulty test pattern has the SLAT property if there exists a fault in the circuit, which is able to reproduce the exact failure behavior observed for this pattern. Therefore, these SLAT-based diagnostic solutions are not guaranteed to work under the presence of multiple faults, for which no SLAT pattern is available. While some other approaches account for test response compaction in the diagnosis of multiple faults [4], [5], they are less effective for highly compacted test signatures collected during BIST.

The reuse of BIST resources for system-level test is discussed in [25], [26], [7], where test architectures are presented to assist the analysis of semiconductor failures. The general diagnostic approach of these solutions is to enable the same techniques for logic diagnosis that are commonly used in a BIST manufacturing environment.

III. The Disturbance Function for Fault Pairs

As discussed in [11], as long as the faults are activated independently in different patterns (SLAT patterns), any diagnostic algorithm for single faults can also handle multiple faults reasonably well. Therefore, the diagnostic challenge is to identify faults which become visible simultaneously in the same test pattern(s).

Fig.1 shows the behavior multiple faults may have in a test pattern. In the top half of Fig. 1 faults f_1 and f_2 have *disjoint observation cones*, while in the bottom half faults f_3 and f_4 interact with one another and exhibit *overlapping observation cones* that result from multiple fault mask and reinforcement effects [12].

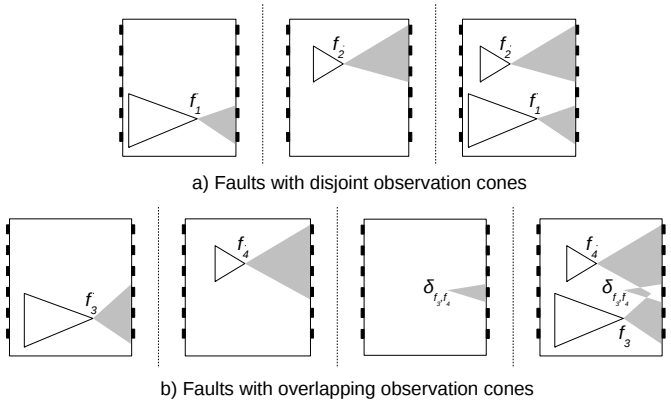

Fig. 1. Disturbance function of a fault pair

For a combinational circuit V with inputs $I := (i_1, i_2, ..., i_p)$ we denote the circuit's fault-free output $V(i_1, i_2, ..., i_p)$, and $V^f(i_1, i_2, ..., i_p)$ is the faulty circuit function in the presence of fault f. The error function introduced by f is simply $D^f(i_1, i_2, ..., i_p) := V(i_1, i_2, ..., i_p) \oplus V^f(i_1, i_2, ..., i_p)$. For variables outside the observation cone the outputs of D^f are constant 0.

For independent faults f_1 and f_2, shown at the top of Fig. 1, the error function D^{f_1,f_2} introduced by the fault pair is

$$D^{f_1,f_2} := D^{f_1} \oplus D^{f_2} = D^{f_1} \vee D^{f_2}$$

since the output variables that equal 1 are disjoint.

For faults f_3 and f_4 with overlapping output cones, shown at the bottom of Fig. 1, a disturbance function δ_{f_3,f_4} is defined as:

$$\delta_{f_3,f_4} := D^{f_3,f_4} \oplus (D^{f_3} \oplus D^{f_4}) \tag{1}$$

The complexity of the disturbance function δ_{f_x,f_y} for any fault pair f_x and f_y will be used later on as a measure for selecting f_x and f_y as multiple fault candidates.

The pairwise definition of a disturbance function describes whether the conditional fault effect of the pair f_x, f_y can be constructed by linear superposition of the respective single fault effects. If the output cones of f_x and f_y are disjoint, this is surely true as $\delta_{f_x,f_y} = 0$. The definition is extended to a set of faults F by

$$\delta_F := D^F \oplus \bigoplus_{f \in F} (D^f) \tag{2}$$

Faults within a fanout-free region may be subject to stronger interdependencies. For example, fault f may *dominate* another fault g so that the effect of g never becomes visible. Alternatively, the effects of f and g may be identical to that of a single fault at their fanout node. In this paper, we focus on identifying the fanout node of a faulty gate, while the location of faults within a fanout-free region are left for subsequent analysis once the chip is available for additional tests.

IV. Direct Diagnosis for Multiple Faults

State-of-the-art approaches for signature-based diagnosis [6], [23], [8] rely on the simulation of single faults to explain the observed signatures obtained from the device under diagnosis (DUD) as introduced in SLAT [24]. However, when multiple faults are present in the device, many signatures do not provide any diagnostic information as they cannot be explained by any single fault. The goal of the developed methodology is to take full advantage of the diagnostic properties of the BIST test set by explaining the largest amount of signatures produced by non-SLAT patterns.

The algorithm presented in this section avoids the exponential computational effort to simulate every possible set of activation conditions in the fault set. Instead, we make use of the linear properties of a MISR compactor and analyze the combination of a fixed number of faulty signatures resulting from the simulation of single faults. These signatures are superimposed and compared to the observed faulty signatures recovered from the DUD.

If a set F of faults has pairwise disjoint output cones, it can be seen from Fig. 1 that δ_F in formula 2 will be constant 0. For the sake of simplicity, we assume a signature-based

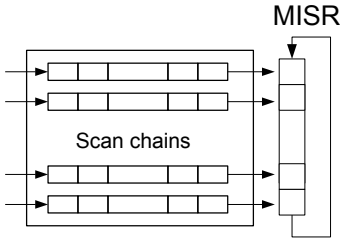

Fig. 2. Signature-based compaction scheme

compaction scheme as shown in Fig. 2 like STUMPS [27], e.g.,

Since linear superposition can be applied for disjoint output cones also in STUMPS, errors in the observed signature are the aggregation of the independent signature errors produced by each fault in F. As the activation conditions are not known beforehand, the signature is explained by solving a linear system of equations. Conversely, if the active faults have overlapping observation cones, we have to add the disturbance function that accounts for all overlapping outputs. This is achieved by compacting the disturbance function δ into a signature error. With this additional function, the observed faulty signature can also be represented as a linear combination of independent error signatures. This approach is an extension of the idea of *partially curable vectors* presented in [28] for semiconductor debug and later in [10] for logic diagnosis.

The entire test consists of multiple sessions, each producing its own signature. The number of signatures which a fault is able to explain, either by itself or in combination with another faults, is a measure of the fault's likelihood. That is, the more signatures a fault explains, the more likely it is considered to represent a faulty chip location.

In the next sub-sections, the procedure to explain observed faulty signatures and rank fault candidates is explained in more detail. The last sub-section presents a complete diagnostic algorithm for multiple faults, together with a short illustrative example.

A. Explaining Non-SLAT Signatures

Let *m* be the longest scan chain in the circuit and *n* the size of the MISR. The state transition function of the MISR is denoted by L.

Assume the DUD's fault free output response is $V := [v_0, v_1, \cdots, v_m]$, where v_t represents the DUD's outputs in scan cycle t. If the MISR is initialized with the all-zero state, the fault free signature S is described by the equation:

$$S := \sum_{i=1}^{m} L^{\,m-i}\, v_i \tag{3}$$

We assume further that a maximum number of q faults are present in the circuit. The observed signature produced by faults $\widetilde{f}_1, \cdots, \widetilde{f}_q$ is $S^{\widetilde{f}_1,\cdots,\widetilde{f}_q}$.

The response error of a fault f is $D^f := [d_0^f, d_1^f, \cdots, d_m^f]$, as already defined above:

$$D^f := V^f \oplus V.$$

Similarly, the signature error E^f of fault f is defined as

$$E^f := S^f \oplus S \tag{4}$$

where S^f if the faulty signature produced by fault f and S is the fault-free signature.

The relation between D^f and E^f is given by

$$E^f := \sum_{i=1}^{m} L^{\,m-i}\, d_i^f \tag{5}$$

In order to explain an observed signature error $E^{\widetilde{f}_1,\cdots,\widetilde{f}_q}$ due to the activation of q faults, we combine the effects of the faults in the *candidate fault set* $C = \{f_1, \cdots, f_k\}$.

An observed signature is explained if the following system of linear equations has a solution:

$$E^{\widetilde{f}_1,\cdots,\widetilde{f}_q} := \begin{bmatrix} E^{f_1} & E^{f_2} & \cdots & E^{f_k} \end{bmatrix} \begin{bmatrix} c_1 \\ c_2 \\ \vdots \\ c_k \end{bmatrix} \tag{6}$$

where the constants $c_1, c_2, \cdots, c_k \in \{0, 1\}$ represent the activation conditions for the faults $f_1, f_2, \cdots, f_k$, respectively, according to the conditional fault model introduced above. Evidently, the interdependencies between $\widetilde{f}_1, \cdots, \widetilde{f}_q$ determine which combination (if any) of faults is able to explain an observed signature.

In the next sub-sections, we present sufficient conditions which guarantee a solution for equation (6).

1) Faults with disjoint observation outputs: The real response error is

$$D^{\widetilde{f}_1,\cdots,\widetilde{f}_q} := c_1 D^{\widetilde{f}_1} \oplus c_2 D^{\widetilde{f}_2} \oplus \cdots \oplus c_q D^{\widetilde{f}_q} \tag{7}$$

After applying linear superposition the error response is

$$E^{\widetilde{f}_1,\cdots,\widetilde{f}_q} := c_1 E^{\widetilde{f}_1} \oplus c_2 E^{\widetilde{f}_2} \oplus \cdots \oplus c_q E^{\widetilde{f}_q} \tag{8}$$

Now, if the candidate set C contains for each active real faults $\widetilde{f}_i$ a representative candidate f_i producing the same signature as $\widetilde{f}_i$, we can substitute the right hand side of equation 8 and find a solution for:

$$E^{\widetilde{f}_1,\cdots,\widetilde{f}_q} := c_1 E^{f_1} \oplus \cdots \oplus c_q E^{f_q} \oplus c_{q+1} E^{f_{q+1}} \cdots \oplus c_k E^{f_k} \tag{9}$$

where $c_i = 0$ for $i > q$.

2) Faults with overlapping observation outputs: The output response error can be expressed as the combination of q and a disturbance function δ:

$$D^{\widetilde{f}_1,\cdots,\widetilde{f}_q} := c_1 D^{\widetilde{f}_1} \oplus c_2 D^{\widetilde{f}_2} \oplus \cdots \oplus c_q D^{\widetilde{f}_q} \oplus \delta \tag{10}$$

The disturbance output can be compacted like any response. If C contains for each active real faults $\widetilde{f}_i$ a representative fault f_i, the following equivalent system of equations has a solution:

$$E^{\widetilde{f}_1,\cdots,\widetilde{f}_q} := c_1 E^{f_1} \oplus c_2 E^{f_2} \oplus \cdots \oplus c_{k-1} E^{k-1} \oplus c_\delta E^{\delta} \tag{11}$$

What remains is to identify the disturbance function δ and the disturbance signature E^{δ}. Let C be the candidate fault set

for solving (11). Without any restriction on E^{δ} (11) would be solvable for any candidate set and would not provide any information. However, we know that δ can only be active at shared outputs of different faults in C. Hence, we search a fault location $f_{\delta} \in F \backslash C$ in the shared logic which can affect shared outputs and only check if (11) is solvable for $E^{\delta} := E^{f_{\delta}}$. If this is the case, we store all the different candidate fault sets together with the auxiliary fault f_{δ}.

B. Fault Ranking

The signature matching procedure presented above identifies sets of active faults $A_{\widetilde{S}} \subset C$ that explains a faulty observed signature $\widetilde{S}$. A set of active faults can be derived as follows:

$$f_i \in A_{\widetilde{S}} \implies \begin{cases} \text{equation (6) is solvable and} \\ c_i = 1 \text{ in equation (6)} \end{cases} \tag{12}$$

The number of signatures $\widetilde{S}$ where $f \in A_{\widetilde{S}}$ is a measure of the fault's *evidence*. That is, the higher this number is, the more likely f is in fact the real cause of the defect behavior. With this criterion, a ranked fault list can be created for logic diagnosis as follows. Let F be the total set of conditional stuck-at faults in the DUD.

A mapping $evidence : F \rightarrow \mathbb{N}_0$ is defined as

$$evidence(f) := |\{\widetilde{S} | f \in A_{\widetilde{S}}\}| \tag{13}$$

The faults f_i are ordered according to decreasing values of $evidence(f_i)$. If there are two faults f_1 and f_2 with $evidence(f_1) = evidence(f_2)$ we prefer the fault sensitized less often.

C. Diagnostic Procedure

The goal of the diagnostic procedure is to identify one or a few suitable fault candidates for each of the defects in the DUD. In the presence of multiple faults several candidates need to be selected to account for all errors in the complete pattern set. For this purpose, candidates that explain a given subset of test patterns are grouped together into the same fault list. Fault lists are constructed from the set of most likely candidate faults C. A few diagnostic candidates are then selected from each fault list in order to identify the final diagnostic candidates that account for the complete observed error behavior.

Initial fault candidates are identified by means of SLAT diagnosis performed on all collected signatures. The outcome of SLAT diagnosis is a set of faults where each fault explains at least one pattern (*splats* in [24]). This set is partitioned into several fault lists as follows:

- Two faults belong to the same list if they explain at least one common pattern
- A given fault can only belong to a single list
- Faults in the same list are ordered according to the procedure described in section IV-B

As shown in Algorithm 1, non-SLAT signatures are explained iteratively (lines 2-14). After initial SLAT diagnosis, the procedure is repeated Q times. One or more fault lists may be created in each iteration and more candidate faults are identified, which may explain other faulty signatures later on. In each iteration, for each unexplained signature we define the fault set C' that contains the best $k-1$ faults from the fault lists so that $E^{f_1}, E^{f_2}, \cdots, E^{f_{k-1}}$ are different and non-zero (line 4). k is a user-defined parameter that fixes the maximum number of free variables in equation (6). In order to assure that, even when all faults are active, equation (6) has a solution, k must be greater than the number of expected faults in the circuit. Note that if $r < k$ faults are active, equation (6) may still have a solution with $c_i = 0$ for $r < i \leq k$. However, k should not be set too high, as equation (6) may become underdetermined.

In line 7 equation (6) is solved for each $f_j \in F \setminus C'$. If a solution is found and f_j is active, the evidence of fault f_j is updated (lines 8-10). Additionally, if there is no suitable candidate list for f_j so far, a new list is generated to be used in the next iteration (line 10). After the faulty signatures have been explained, the candidates with higher evidence in each list are selected as the final diagnostic candidates (line 15).

Algorithm 1 Diagnostic Procedure

```
1:  SLAT diagnosis
2:  for 1 → Q do
3:    for all unmatched signatures do
4:      C' := select k−1 candidate faults from the fault lists
5:      for all f_j ∈ F \ C' do
6:        C := C' ⋃ f_j
7:        Solve equation (6)
8:        if equation 6 has a solution and f_j is active then
9:          Update evidence for f_j
10:         Update fault lists
11:       end if
12:     end for
13:   end for
14: end for
15: Fault Ranking
```

Note that solving equation (6) allows the identification of faults for which no SLAT pattern is present in the test set. For example, Figures 3 and 4 show a circuit affected by two faults a and b. As Fig. 3 shows, fault a can directly explain the signatures corresponding to SLAT patterns 1 and 2, while b by itself cannot explain any SLAT pattern. Moreover, the disturbance function f_{δ} explains only one of the two signatures explained by fault a and affects only circuit output o. Consequently, a single fault list is generated, which includes both faults a and f_{δ}.

As Fig. 4 shows, mask and reinforcement effects between faults a and b are observed for pattern 3 only in output o. This non-SLAT pattern can be explained if C contains faults a, b and the auxiliary fault f_{δ} corresponding to the disturbance function. Thus, a new ranked fault list can be created for b and, therefore, b can be identified as a possible fault candidate.

In this diagnostic procedure the fault signatures can be calculated on-the-fly or precomputed and stored beforehand. In this case, the only computational effort amounts to the solution of linear systems of equations. The effectiveness of the procedure is affected by the number of iterations Q. However, experimental results show that for $Q \leq 2$ most faulty signatures can already be explained.

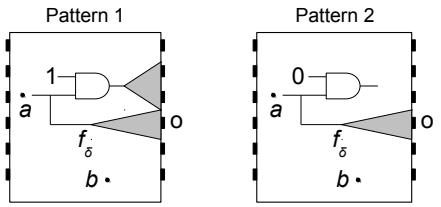

Fig. 3. SLAT patterns

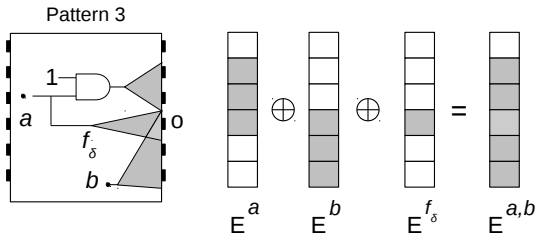

Fig. 4. Non-SLAT pattern

V. Experimental Results

In order to validate the proposed approach, experiments with industrial circuits provided by NXP were carried out. Both pseudo-random and deterministic patterns are used: a sequence of 10000 pseudo-random patterns is applied first and, for the hard-to-detect faults, ATPG patterns are applied. Each test pattern is compacted into a 32-bit signature using a MISR. Algorithm 1 is executed for two iterations ($Q = 2$) and 10 faults in the candidate set ($k = 10$). The characteristics of the circuits, the pattern sets and the achieved fault coverages are shown in Table I.

Circuit	#gates	stuck-at faults	# of patterns	Fault coverage
p45k	38811	71848	11746	99.69 %
p100k	84356	162129	10386	99.56 %
p141k	152808	283548	10670	98.86 %
p239k	224597	455992	10571	98.84 %
p259k	298796	607536	10736	99.10 %
p267k	239687	366871	10641	99.60 %
p269k	239771	371209	10642	99.60 %
p279k	257736	493844	10920	97.89 %
p286k	332726	648044	11311	98.34 %
p295k	249747	472124	12086	99.15 %
p330k	312666	540758	15530	98.95 %

TABLE I. Circuit characteristics

For each diagnostic experiment, a set of 5 faults is activated with a probability p ranging from 0.05 to 1.0, where a probability of 1.0 corresponds to the activation of multiple stuck-at faults. Additionally, in order to consider mask and reinforcement effects between injected faults, we perform two sets of experiments. In the *uniform* experimental setup, the location of the faults are chosen randomly, while in the *topological* setup, faults are injected within the input or output cone of a randomly chosen location in the circuit.

For each circuit, a total of 600 diagnostic experiments have been conducted. We consider a fault is correctly diagnosed if the corresponding node appears in the top five candidates of any of the candidate lists. Diagnostic accuracy is defined as the percentage of correctly diagnosed faults out of all injected faults.

design	uniform setup		topological setup	
	SLAT	proposed	SLAT	proposed
p45k	53.13 %	99.99 %	64.35 %	98.84 %
p100k	66.16 %	100.00 %	56.61 %	98.27 %
p141k	58.11 %	99.99 %	60.10 %	98.59 %
p239k	51.37 %	99.91 %	59.24 %	98.04 %
p259k	61.44 %	99.99 %	49.18 %	99.61 %
p267k	59.41 %	99.98 %	49.07 %	99.33 %
p269k	59.90 %	99.99 %	60.88 %	99.47 %
p279k	64.34 %	99.89 %	71.22 %	98.83 %
p286k	67.83 %	99.97 %	56.90 %	97.77 %
p295k	63.27 %	98.01 %	68.86 %	98.92 %
p330k	66.83 %	99.94 %	62.98 %	96.81 %

TABLE II. Percentage (%) of explained faulty patterns

Table II shows the percentage of explained patterns in the test set for both experimental setups. Columns two and four in Table II show the percentage of SLAT patterns for the uniform and topological test setups, respectively, while columns three and five show the number of explained patterns with the developed approach. Almost all faulty signatures provide some useful diagnostic information for the presented approach, while any SLAT-based method can only account for roughly 60 % of the faulty test responses.

Table III compares the average diagnostic accuracy over all activation probabilities. Columns two and three show diagnostic results for the uniform setup while columns four and five present those of the topological setup. Columns two and four show the outcome of the SLAT approach while columns three and five account for the procedure presented in this paper. These results show the presented signature-based approach achieves an average accuracy improvement of over 10% when compared to state-of-the-art SLAT solutions.

Design	Uniform setup		Topological setup	
	SLAT	Proposed	SLAT	Proposed
p45k	79.53 %	97.03 %	78.16 %	90.05 %
p100k	82.67 %	97.52 %	73.64 %	85.94 %
p141k	90.16 %	100.00 %	87.73 %	96.06 %
p239k	85.48 %	97.75 %	82.84 %	93.82 %
p259k	93.04 %	98.79 %	86.02 %	95.98 %
p267k	83.57 %	97.84 %	85.28 %	97.32 %
p269k	87.89 %	99.07 %	80.58 %	95.07 %
p279k	79.87 %	97.32 %	76.60 %	91.49 %
p286k	87.25 %	97.79 %	84.93 %	97.26 %
p295k	86.67 %	98.92 %	79.66 %	95.86 %
p330k	86.35 %	97.77 %	76.35 %	89.97 %

TABLE III. Average diagnostic accuracy

Table IV below gives a more detailed insight and shows the diagnostic accuracy of the new methodology for activation probabilities of 0.05 and 1.0 separately. The presented approach is efficient for both low activation probability and deterministic activation $p = 1.0$. In both cases it outperforms SLAT significantly. The table also shows that the performance of the SLAT approach improves for a larger activation probability. This is due to the fact that the more often faults are activated, the more likely it is that at least one SLAT pattern exists for each fault and, therefore, it can be easily diagnosed. Unsurprisingly, the topological setup is the most difficult to diagnose. In particular, the performance of the SLAT approach is lowest for this setup with $p = 0.05$. The accuracy in this case is improved on average by 16 %.

The greatest improvement is achieved for circuit p279k where the improvement by the presented approach is 22.5 %.

Design	SLAT				Proposed			
	uniform setup		topological setup		uniform setup		topological setup	
	$p = 0.05$	$p = 1.0$	$p = 0.05$	$p = 1.0$	$p = 0.05$	$p = 1.0$	$p = 0.05$	$p = 1.0$
p45k	57.73 %	91.95 %	76.06 %	78.00 %	90.91 %	100.00 %	94.37 %	87.00 %
p100k	72.00 %	87.93 %	67.16 %	83.87 %	97.33 %	97.41 %	85.07 %	90.32 %
p141k	81.82 %	92.31 %	86.57 %	82.86 %	100.00 %	100.00 %	98.51 %	94.29 %
p239k	81.82 %	91.23 %	67.86 %	88.51 %	96.59 %	100.00 %	89.29 %	93.10 %
p259k	90.12 %	98.18 %	81.16 %	91.07 %	98.77 %	100.00 %	92.75 %	99.11 %
p267k	73.68 %	87.23 %	78.57 %	88.10 %	92.11 %	94.95 %	85.71 %	96.43 %
p269k	91.89 %	90.43 %	77.42 %	83.84 %	100.00 %	100.00 %	100.00 %	95.96 %
p279k	75.00 %	81.63 %	75.00 %	88.46 %	97.22 %	97.96 %	86.11 %	93.59 %
p286k	82.35 %	93.94 %	78.85 %	92.59 %	98.53 %	96.97 %	100.00 %	98.77 %
p295k	80.56 %	87.23 %	79.59 %	84.62 %	100.00 %	99.20 %	95.92 %	96.70 %
p330k	80.00 %	94.06 %	72.00 %	77.22 %	96.00 %	100.00 %	96.00 %	87.34 %

TABLE IV. Diagnostic accuracy for $p = 0.05$ and $p = 1.0$

Finally, the runtime of the diagnostic procedure is on average 76 seconds. For circuits p45k and p330k the runtimes amount roughly to 12 and 189 seconds, respectively.

VI. Conclusion

In this paper a diagnostic procedure for the analysis of multiple faults is presented by using compacted test signatures collected from the faulty integrated circuit. The developed approach makes use of the linear properties of a MISR compactor in order to analyze the simultaneous activation of several faults without exhaustive fault simulation. In contrast to previous approaches, experimental results show that the presented technique takes advantage of almost all faulty patterns in the test set. Diagnostic accuracy is improved by up to 22% and in average by more than 16% when compared to state-of-the-art approaches in the literature.

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