Built-in Self-Diagnosis Targeting Arbitrary Defects with Partial Pseudo-Exhaustive Test

Cook, Alejandro; Hellebrand, Sybille; Imhof, Michael E.; Mumtaz, Abdullah; Wunderlich, Hans-Joachim

Proceedings of the 13th IEEE Latin-American Test Workshop (LATW'12) Quito, Ecuador, 10-13 April 2012

doi: http://dx.doi.org/10.1109/LATW.2012.6261229

Abstract: Pseudo-exhaustive test completely verifies all output functions of a combinational circuit, which provides a high coverage of non-target faults and allows an efficient on-chip implementation. To avoid long test times caused by large output cones, partial pseudo-exhaustive test (P-PET) has been proposed recently. Here only cones with a limited number of inputs are tested exhaustively, and the remaining faults are targeted with deterministic patterns. Using P-PET patterns for built-in diagnosis, however, is challenging because of the large amount of associated response data. This paper presents a built-in diagnosis scheme which only relies on sparsely distributed data in the response sequence, but still preserves the benefits of P-PET.

Preprint

Built-in Self-Diagnosis Targeting Arbitrary Defects with Partial Pseudo-Exhaustive Test

Alejandro Cook[1], Sybille Hellebrand[2], Michael E. Imhof[1], Abdullah Mumtaz[1], Hans-Joachim Wunderlich[1]
[1]Institute of Computer Architecture and Computer Engineering, University of Stuttgart, Germany
E-mail: {cook, imhof, mumtazah}@iti.uni-stuttgart.de, wu@informatik.uni-stuttgart.de
[2]Institute of Electrical Engineering and Information Technology, University of Paderborn, Germany
E-mail: sybille.hellebrand@uni-paderborn.de

Abstract—**Pseudo-exhaustive test completely verifies all output functions of a combinational circuit, which provides a high coverage of non-target faults and allows an efficient on-chip implementation. To avoid long test times caused by large output cones, partial pseudo-exhaustive test (P-PET) has been proposed recently. Here only cones with a limited number of inputs are tested exhaustively, and the remaining faults are targeted with deterministic patterns. Using P-PET patterns for built-in diagnosis, however, is challenging because of the large amount of associated response data. This paper presents a built-in diagnosis scheme which only relies on sparsely distributed data in the response sequence, but still preserves the benefits of P-PET.**

***Index Terms*—Built-in Self-Test, Pseudo-Exhaustive Test, Built-in Self-Diagnosis**

I. Introduction

Pseudo-exhaustive testing (PET) was proposed in the 1980's to guarantee high defect coverage by a simple test generation process also suitable for on-chip implementation [2][8]. Given a circuit with inputs I and outputs O, for each output $o \in O$ the set $I(o) \subset I$ contains all inputs the output o depends on. A pseudo-exhaustive test applies all possible input combinations for each input set $I(o)$. Serially exercising all input sets requires at most $|O| \cdot 2^w$ test patterns, where w is the cardinality of the largest input set. Thus, a PET is only feasible, if w does not exceed a given limit, e.g. $w = 24$.

Meanwhile PET has regained attention, because its high defect coverage independent of specific fault models is particularly attractive in the presence of new defect mechanisms in nanoscale technologies. Furthermore, today's high speed circuits are characterized by limited circuit depths and, consequently, by smaller input sets $I(o)$. Recently, partial pseudo-exhaustive test (P-PET) has been proposed as a solution for arbitrary circuits [9]. Here, exhaustive patterns are applied only to inputs sets of limited size $|I(o)| \leq b$. This way large parts of the circuit can be exhaustively covered, and for the remaining parts, the generated patterns provide high quality random patterns. Compared to a mixed-mode BIST using pseudo-random patterns, a P-PET complemented with deterministic patterns can provide higher defect coverage with less test data storage.

To exploit the benefits of P-PET also for yield ramp-up and in-field repair, it must be combined with efficient techniques for built-in self-diagnosis (BISD). Built-in diagnosis has been in the focus of research for many years, but most of the approaches either require multiple test runs or are not compatible with a standard scan architecture. The window-based diagnosis in [4][5] is compatible with STUMPS and supports a fully autonomous BISD in a single test run. Nevertheless, applying this scheme to long test sequences would result in very high storage requirements for the response data. BISD for LBIST and for mixed-mode BIST with long pseudo-random sequences needs additional strategies for reducing the response data [1][6]. As the sequences for P-PET are typically much longer than the pseudo-random sequences in LBIST or mixed-mode BIST, it is even more challenging to limit the storage requirements for response data. This paper shows how the diagnosis approach in [5] can be adapted to efficiently deal with P-PET sequences while maintaining the high defect coverage.

II. Architecture

As shown in Figure 1 the P-PET architecture proposed in [9] is combined with the window-based diagnosis of [4][5]. To generate a P-PET sequence for a given bound b, the multiple-polynomial LFSR (MP-LFSR) switches between several polynomials stored on chip, each one exercising a subset of $I_b = \{I(o) \mid |I(o)| \leq b\}$, such that overall each input set in I_b receives all possible input combinations. The polynomials are pre-computed relying on the check criterion described in [2]. Deterministic patterns are added to cover those faults, which are not detected by the P-PET sequence. During test, the MP-LFSR is used as a decompressor to regenerate the patterns from the respective seeds stored in the seed memory.

This work has been performed within the project RealTest sponsored by the German National Science Foundation (DFG-grants HE 1686/3-2 and WU 245/5-2).

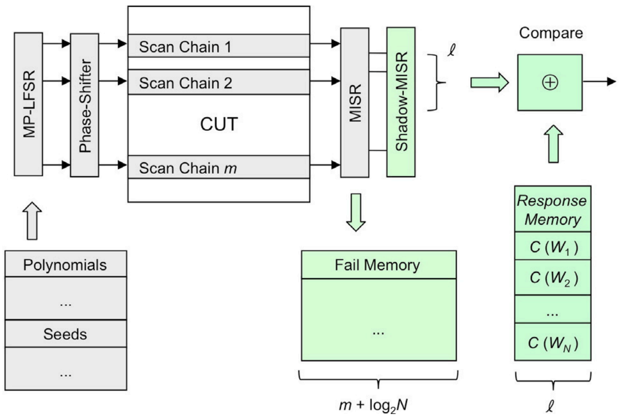

Figure 1. Figure 1: Architecture for BISD with P-PET

For diagnosis the test is partitioned into windows, i.e. short contiguous test sequences. Each window is characterized by a single cumulative signature, which is copied to a shadow-MISR at the end of the window. While the test continues normally with the next window, the shadow MISR runs in autonomous mode as long as the first pattern is applied. This way fault effects are distributed over the MISR randomly, and it is sufficient to observe only ℓ bits of the shadow-MISR [5]. The observed bits are compared to the respective reference data stored in the response memory. If a mismatch is detected, the complete signature is stored in the fail memory together with the index of the test window.

III. Diagnosis

The window-based diagnosis proposed in [4][5] is based on the conditional stuck-at fault model and computes the fault location directly from the faulty signature. While other schemes for "direct diagnosis" analyze signatures for single patterns [3], here signatures correspond to windows in the test sequence. For each candidate fault location v, the circuit responses are determined when a stuck-at-zero or stuck-at-one fault at v is activated by a single pattern in the window. From this information a system of linear equations is built, which has a solution, only if the fault location v explains the faulty behavior. To support a unique solution, the dimensions of the system of equations must be properly set. As shown in [4][5], the number of patterns in a window should be less than or equal to the number of bits in the MISR signature. A straightforward application of the scheme to long P-PET sequences would therefore result in an extremely large response memory.

To reduce the response data and keep the high defect coverage, the P-PET sequence is partitioned into "strong" and "weak" diagnostic windows similarly as in [6]. "Strong" windows fulfill the length restrictions of [4][5] and are analyzed with the corresponding approach. "Weak" windows can contain more patterns and are treated with a less expensive diagnostic procedure.

For partitioning the P-PET sequence $T_{P\text{-}PET}$ into strong and weak windows, it is first fault-simulated against a given set of target faults F. Whenever a fault is detected for the first time, the respective pattern is stored in the set of candidate essential patterns $E(T_{P\text{-}PET})$. Subsequently, ATPG-patterns T_{det} are generated for the undetected hard faults. Then the candidate essential patterns and the deterministic patterns $E(T_{P\text{-}PET}) \cup T_{det}$ are fault simulated in reverse order, and unnecessary patterns are dropped. This way a reduced set of deterministic patterns T^*_{det} and the set $E^*(T_{P\text{-}PET})$ of essential P-PET patterns are obtained. Each essential pattern in $E^*(T_{P\text{-}PET})$ corresponds to a strong diagnostic window of length $n = 2^k$ as follows: The complete sequence $T_{P\text{-}PET}$ is divided into windows of length $n = 2^k$. If a window contains an essential pattern, it is called a strong diagnostic window. The windows between two strong windows are joined into one weak diagnostic window. Overall the window structure shown in Figure 2 is obtained, i.e. the strong windows are positioned around the essential patterns, such that the starting index of a window is always a multiple of 2^k.

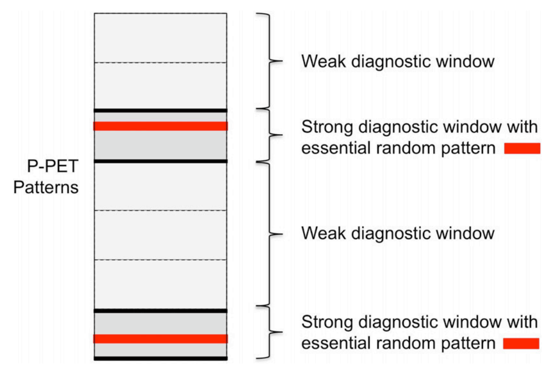

Figure 2. Figure 2: Partitioning a P-PET sequence into diagnostic windows.

Finally, the deterministic patterns T^*_{det} are divided into diagnostic windows of size 2^k, which are also referred to as strong windows.

If faulty signatures appear at the end of both weak and strong windows, then the procedure described in [4][5] is applied to the strong windows only. The patterns in the weak windows are fault simulated to validate the results or to resolve ambiguities. If a faulty signature is observed only at the end of a weak window, then the direct diagnosis procedure described in [7] is applied.

IV. Experimental Results

The proposed P-PET diagnosis has been evaluated for a set of industrial circuits kindly provided by NXP. The circuit characteristics are listed in Table I. In all experiments reported below, 32-bit MISRs are used, and strong diagnostic windows always contain 32 patterns.

TABLE I. CIRCUIT CHARACTERISTICS

Circuit	*#Gates*	*#Scan FFs*	*#Scan Chains*	*Max. Length*	*# Stuck-at Faults*
p45k	38811	2250	333	97	71848
p100k	84356	5829	270	53	162129
p141k	152808	10502	264	45	283548
p239k	224597	18495	260	61	455992
p267k	239687	16621	260	62	366871
p269k	239771	16621	360	62	371209
p279k	257736	17835	385	59	493844
p295k	249747	18521	330	62	472124
p330k	312666	18468	320	64	540758

The P-PET approach is compared to a mixed-mode BIST with 4096 and 100000 pseudo-random patterns. Table II shows the achieved fault coverage and compares the cost of deterministic patterns both in terms of the number of patterns and the number of specified bits. The number of specified bits is used as an estimate for the seed memory. As Table II shows, the P-PET scheme greatly reduces the storage requirements for deterministic patterns.

TABLE II. COST OF DETERMINISTIC PATTERNS

Circuit	*Fault Coverage*	*# Patterns / # Specified Bits*		
		4096 PRP	*100000 PRP*	*P-PET (b = 24)*
p45k	99.70%	1940 / 52068	303 / 9064	16 / 1011
p100k	99.56%	414 / 60539	118 / 18843	14 / 1574
p141k	98.85%	704 / 375597	494 / 254410	219 / 71078
p239k	98.84%	618 / 162221	431 / 102537	180 / 18238
p267k	99.60%	678 / 393979	578 / 325800	434 / 225732
p269k	99.58%	693 / 396025	533 / 322150	433 / 227091
p279k	97.89%	917 / 397743	668 / 279820	343 / 149583
p295k	99.15%	2553 / 579146	748 / 362839	662 / 230737
p330k	98.95%	5587 / 986122	5191 / 866846	4490 / 699460

Table III presents the response data for the P-PET approach as well as the overall memory cost for seed and response data. For comparison Table IV shows the size of the seed memory (SM), the response memory (RM), as well as the overall memory cost (Σ) in bytes also for a mixed-mode BIST with 4096 and 100000 pseudo-random patterns. For circuits p141k and p330k P-PET has the lowest overall cost. Although the overall cost for P-PET is higher for the other circuits, it can be observed that the reduction in seed memory can compensate the growing response memory to a large extent and keep it in a feasible range. Furthermore, as

TABLE III. TEST AND RESPONSE DATA FOR P-PET ($\ell = 8$, b=24)

Circuit	*# Strong Windows*	*# Weak Windows*	*Control Data [Byte]*	*Overall Response Data [Byte]*	*Seed + Response Data [Byte]*
p45k	1844	1029	4841	7714	7841
p100k	2001	1239	5253	8493	8690
p141k	3560	2847	9790	16197	25082
p239k	3928	3046	10802	17776	20056
p267k	3731	2801	10261	16793	45010
p269k	3746	2795	10302	16843	45230
p279k	5179	3794	14243	23216	41914
p295k	7730	5397	21258	34385	63228
p330k	3250	3949	9344	16343	103776

TABLE IV. COMPARISON OF OVERALL COST [BYTE]

Circuit	*Mixed-Mode BIST with 4096 PRP*			*Mixed-Mode BIST with 100000 PRP*		
	SM	RM	Σ	SM	RM	Σ
p45k	6509	189	6698	1133	3680	4813
p100k	7568	141	7709	2356	2251	4607
p141k	46950	150	47100	31802	2177	33979
p239k	20278	148	20426	12818	2320	15138
p267k	49248	150	49398	40725	2212	42937
p269k	49504	150	49654	40269	2218	42487
p279k	49718	157	49875	34978	2760	37738
p295k	72394	208	72602	45355	3381	48736
p330k	123266	303	123569	108356	2114	110470

shown in Table VI, the coverage of non-target faults increases for the P-PET approach.

In order to analyze the diagnostic accuracy, a total of 400 faults have been randomly and uniformly injected into each circuit. The fault set consists of 100 stuck-at faults, 100 crosstalk faults, 100 delay, and 100 wired-AND faults. A fault is considered as correctly diagnosed, if it is one of the top 5 fault candidates in the ranked list after the responses in the fail memory have been analyzed. The depth of the fail memory has been set to 100. Table V shows the results. The last column shows the improvement due to the additional analysis of weak windows. The same experiment for a mixed-mode BIST with 4096 and 100000 pseudo-random patterns achieved a lower or equal diagnostic resolution for the non-target faults in all cases. Concerning stuck-at faults, the higher number of deterministic stuck-at patterns led to a higher diagnostic resolution for p45k and 4096 pseudo-random patterns.

Finally, Table VI illustrates the contribution of the strong and weak windows to the detection of non-target faults. The column “Strong” reports the number of undetected faults, if only the patterns in the strong windows are evaluated (the mixed-mode BIST with the short pseudo-random sequence is partitioned into strong windows only). The column “Stong+Weak” lists the number of undetected faults, for the complete test.

TABLE V. DIAGNOSTIC RESOLUTION AND IMPACT OF WEAK WINDOWS

Circuit	***Stuck-At***	***Cross-talk***	***Delay***	***Wired-And***	***Improve-ment by weak windows***
p45k	99	89	96	91	6
p100k	98	93	95	100	3
p141k	99	89	91	95	6
p239k	98	95	93	100	3
p267k	99	86	93	95	0
p269k	98	90	92	99	3
p279k	95	85	90	94	0
p295k	95	80	80	86	2
p330k	95	90	89	94	2

TABLE VI. UNDETECTED NON-TARGET FAULTS

Circuit	***4096 PRP Strong***	***100000 PRP***		***P-PET***	
		Strong	***Strong + Weak***	***Strong***	***Strong + Weak***
p45k	36	31	27	25	11
p100k	17	10	7	10	3
p141k	26	23	20	15	6
p239k	18	11	9	10	6
p267k	34	23	20	20	8
p269k	32	16	16	14	4
p279k	35	21	21	18	10
p295k	52	42	42	38	38
p330k	29	26	23	21	13

Comparing the results shows that the weak windows maintain the defect coverage as expected and P-PET has the highest defect coverage.

V. CONCLUSIONS

Partial pseudo-exhaustive test offers a high coverage of non-target faults and considerably reduces the storage requirements for deterministic patterns. Partitioning a P-PET sequence into strong and weak diagnostic windows supports a fully autonomous BISD combining the high defect coverage with a high diagnostic resolution for non-target faults as well as feasible storage requirements.

REFERENCES

[1] M. E. Amyeen et al., "Logic BIST Silicon Debug and Volume Diagnosis Methodology," Proc. IEEE Int. Test Conf. (ITC'11), Anaheim, CA, USA, Sept. 2011, pp. 1-10

[2] Z. Barzilai, D. Coppersmith, A. L. Rosenberg, "Exhaustive Generation of Bit Patterns with Applications to VLSI Self-Testing," IEEE Trans. on Comp., Vol. C-32, No. 2, Feb. 1983, pp. 190- 194.

[3] W.-T. Cheng et al., "Signature based diagnosis for logic BIST," in Proc. IEEE Int. Test Conf. (ITC'06), Santa Clara, CA, USA, 2006, pp. 1-9

[4] A. Cook, M. Elm, H.-J. Wunderlich, U. Abelein, "Structural In-Field Diagnosis for Random Logic Circuits," Proc. Eur. Test Symp. (ETS'11), Trondheim, Norway, May 2011, pp. 111-116

[5] A. Cook, S. Hellebrand, T. Indlekofer, H.-J. Wunderlich, "Diagnostic Test of Robust Circuits," Proc. Asian Test Symp. (ATS'11), New Delhi, India, November 2011.

[6] A. Cook, S. Hellebrand, H.-J. Wunderlich, "Built-in Self-Diagnosis Exploiting Strong Diagnostic Windows in Mixed-Mode Test," Proc. Eur. Test Symp. (ETS'12), Annecy, France, May 2012

[7] S. Holst and H.-J. Wunderlich, "A Diagnosis Algorithm for Extreme Space Compaction," Proc. Design, Automation and Test in Europe (DATE'09), Nice, France, April 20-24, 2009, pp. 1355-1360.

[8] E. J. McCluskey, "Verification Testing - A Pseudoexhaustive Test Technique," IEEE Transactions on Computers, Vol. C-33, No. 6, June 1984, pp. 541 – 546.

[9] A. Mumtaz, M. E. Imhof, H.-J. Wunderlich, "P-PET: Partial Pseudo-Exhaustive Test for High Defect Coverage," Proc. IEEE Int. Test Conf. (ITC'11), Anaheim, CA, USA, Sept. 2011, pp. 1-8