Testing and Monitoring Nanoscale Systems – Challenges and Strategies for Advanced Quality Assurance

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Abstract – The increased number of fabrication defects, spatial and temporal variability of parameters, as well as the growing impact of soft errors in nanoelectronic systems require a paradigm shift in design, verification and test. A robust design becomes mandatory to ensure dependable systems and acceptable yields. Design robustness, however, invalidates many traditional approaches for testing and implies enormous challenges. The RealTest Project addresses these problems for nanoscale CMOS and targets unified design and test strategies to support both a robust design and a coordinated quality assurance after manufacturing and during the lifetime of a system. The paper first gives a short overview of the research activities within the project and then focuses on a first result concerning soft errors in combinational logic. It will be shown that common electrical models for particle strikes in random logic have underestimated the effects on the system behavior. The refined model developed within the RealTest Project predicts about twice as many single events upsets (SEUs) caused by particle strikes as traditional models.

1 INTRODUCTION

Continuously shrinking feature sizes offer a high potential for integrating more and more functionality into a single chip. However, technology scaling also comes along with completely new challenges for design and test. As in the past, manufacturing defects are still a major problem, and efficient test and diagnosis procedures are needed to detect and sort out failing devices. While "random" or "spot" defects, such as shorts or opens, have been the major concern so far, the scenario has changed in the nanoscale era. The increasing variability of transistors, the degradation of devices, as well as the increasing susceptibility to transient faults during system operation lead to massive reliability problems [5, 39].

One major reason for static parameter variations is sub-wavelength lithography. For nanoscale fabrication processes the wavelength used for lithography is greater than the size of the structures to be patterned. As in pictures with a low resolution, the resulting structures don't have exactly the intended contours. Even if techniques for resolution enhancement (RET) such as optical proximity correction (OPC) are applied, these effects cannot be fully compensated [24].

A second source of static variability is the extremely small number of dopant atoms in the channel of a transistor. Although the concentration of dopant atoms in the channel remains more or less constant, the decreasing channel lengths lead to an exponential decrease of the number of dopant atoms with successive technology generations, and below 50 nm only tens of atoms are left. This implies that the "Law of Large Numbers" is no longer valid and disturbances in a few atoms already result in different electric characteristics of the transistors, as for example different threshold voltages. This phenomenon is also referred to as "random dopant fluctuations".

Finally the varying power density in different components of a system is a reason for dynamic parameter variations. Extremely high switching activity in certain areas, e.g. the ALU in a microprocessor, may for example cause "hot spots" which in turn may result in voltage droops and supply voltage variations.

During the lifetime of a chip, aging and degradation of devices can produce new permanent faults, which stay in the system. Transient faults or "soft errors", which affect the system operation for a short time and then disappear again, can be caused by α-particles emitted from the packaging material or by cosmic radiation. Traditionally, soft errors have only been considered for memories, because the more aggressive design rules for SRAM and DRAM arrays made them more susceptible to particle strikes. Meanwhile, a saturation of the soft error rate (SER) in memories can be observed, while the vulnerability of combinational logic and latches is increasing [2, 13].

To cope with these inevitable problems, a "robust" design will become mandatory not only for safety critical applications but also for standard products. On the one hand, a shift from deterministic to statistical design is necessary to deal with parameter variations [5, 39]. On the other hand, fault tolerance and soft error mitigation techniques are necessary to compensate a certain amount of errors [2, 13, 29, 34].

However, the changing design paradigms also require a paradigm shift in test. As "robust" systems are designed to compensate faults to a certain extent, it is no longer sufficient to classify chips into passing and failing chips. Instead, additional information about the remaining robustness of passing chips is required ("quality binning"). Furthermore, the "acceptable" behavior of a system may vary within a certain range, which is possibly application specific (e.g. accuracy or speed). Consequently, test development cannot only be based on classical measures such as fault coverage, but tests have to verify that modules fulfill their specifications including robustness properties. Additional problems arise, because traditional observables such as I_{DDQ} are no longer reliable failure indicators.

2   THE REALTEST PROJECT

The problems explained above are addressed by the RealTest Project, which targets unified design and test strategies supporting both a robust design and efficient test procedures for manufacturing test as well as online test and fault tolerance. The project is a joint initiative of the Universities of Freiburg (Bernd Becker, Ilia Polian), Stuttgart (Hans-Joachim Wunderlich), and Paderborn (Sybille Hellebrand), and the Fraunhofer Institute of Integrated System Design and Design Automation Dresden (Bernd Straube) [4]. It is funded by the German National Science Foundation (DFG) and gets industrial support from Infineon Technologies, Neubiberg, and NXP Semiconductors Hamburg. In detail the research focus is on the following topics:

- Fault modeling,
- State monitoring in complex systems,
- Testing fault tolerant nanoscale systems,
- Modeling, verification and test of acceptable behavior.

The research activities are strongly dependent on each other. To design for example a robust system, which can compensate disturbances during system operation, a detailed analysis of possible defect and error mechanisms is indispensable. This analysis must take into account statistical variations of the circuit parameters and provide a statistical characterization of the resulting behavior. Depending on the results the appropriate design and fault tolerance strategies can be selected. Particular attention must be paid to flip-flops and latches, as they become the dominating components in random logic and are extremely vulnerable. As the known techniques for hardening flip-flops and latches are very costly, new efficient techniques for state monitoring are needed. The design strategy and the data obtained by the initial defect and error analysis determine the constraints for the test of the system. The cost for test and design can be reduced, if it is possible to identify critical and non-critical faults depending on the application. For example, a fault in a DVD player resulting in only a few faulty pixels at certain times is tolerable for the user and need not be considered. A precise and application specific model of the acceptable behavior of the system is the basis for this step.

A short outline of the specific problems dealt with in each topic is given in the following subsections.

2.1 Fault modeling

Defects, soft errors and parameter variations in future technologies cannot be accurately characterized by existing fault models. To be able to deal with the complex physical phenomena responsible for the circuit behavior, new fault models must be developed comprising, in particular, statistical profiles of circuit parameters and conditions for fault detection.

This work is based on techniques for inductive fault analysis, which extract the behavior of defective layouts via the electrical level to higher levels of abstraction [18]. As classical approaches for inductive fault analysis do not take into account spatial and temporal variabilities, they must be extended accordingly. A first result concerning soft errors in combinational logic will be described in Section 3.

2.2   State monitoring in complex systems

The percentage of flip-flops in logic components is rapidly growing, which is for example due to massive pipelining or speculative computing based on large register files. In particular, fault tolerant architectures rely on redundant structures and also work with an increased number of memory elements. Already today, circuits with more than a million flip-flops can be found both in data dominated and in control dominated designs [21].

Flip-flops are particularly susceptible to hard and soft errors, and, as it will be analyzed in more detail in Section 3, soft errors in the combinational logic also propagate to the system flip-flops with a higher probability than assumed so far. An additional problem appears in power aware designs, where clock gating is used to keep the system state for longer periods of time. Similar as the contents of memory arrays, the system state is then exposed to disturbances over longer time spans.

Ensuring the correct system state is thus a problem of major importance. However, while online testing and monitoring of memory arrays is already state of art, respective techniques for logic circuitry are still in their infancy. Here the goal is to investigate monitoring techniques and reconfiguration strategies, which are suitable for both manufacturing and online test. In particular new and robust hardware structures for scan chains are under development. Similar as in memory arrays, the key issue is not to harden each single memory element but to partition the flip-flops

into appropriate subsets, which can be monitored with the help of failure characteristics [14].

2.3 Testing fault tolerant nanoscale systems

On the one hand robust design styles are contradictory to traditional design for testability rules, as they decrease the observability of faults. On the other hand fault masking helps to increase yield. Consequently, a "go/nogo" test result is no longer satisfactory, instead information about the remaining robustness in the presence of faults is needed for quality binning.

As classical fault tolerant architectures such as triple modular redundancy (TMR) are very costly to implement, they are still restricted to safety critical applications [36]. For other systems, less hardware intensive solutions are of particular interest. The research activities within the project therefore focus on self-checking designs, which are able to detect errors and initiate a recovering phase once an error has happened [33]. Typically self-checking systems aim to achieve the totally self-checking goal (TSC), i.e. to detect an error when it results in a wrong output for the first time. Strongly fault secure circuits e.g. achieve the TSC by guaranteeing for each fault either a test pattern or fault free operation even in the case of fault accumulation [40]. Design guidelines for strongly fault secure circuits are already given in [40], more advanced techniques are described in [22].

In principle, tools for automatic test pattern generation (ATPG) can be used to both verify the self-checking properties of the design and to generate test patterns for manufacturing test. Clearly an ATPG tool can verify the existence of test patterns, and checking fault free operation in the presence of faults corresponds to the known problem of redundancy identification. However, there are several challenges, which are not yet addressed in state of the art tools. To deal with fault accumulation, the tools must be able to handle multiple faults efficiently. Furthermore, self-checking designs usually work with input and output encoding, and test patterns for online checking must be in the input code and result in a circuit response outside the output code. This requires ATPG with respective constraints. For manufacturing test, the fault model may be different from that for online checking. The interaction between both fault models must be analyzed, and a test set must be determined which can detect not only manufacturing defects but also reduced self-checking properties.

2.4 Modeling, verification and test of acceptable behavior

As mentioned above, the behavior of nanoscale systems may be "acceptable" within a certain range, which is possibly application specific (e.g. accuracy or speed). This observation has been exploited in [6] to introduce the concept of error tolerant design. Within the framework of the RealTest Project a more general approach is followed to develop metrics for "acceptable behavior" taking into account aspects of both offline and online testing.

Along with the development of respective metrics and their integration into ATPG tools, an important issue is to provide means for estimating the impact of hard or soft errors. The "severity" of a soft error in a sequential circuit can for example be measured by the number of clock cycles the system needs to return to a fault free state [12]. The respective classification of soft errors in [12] is based on a temporary stuck-at fault model for soft errors and an efficient estimation of the error probability P_{err} associated with each fault. P_{err} reflects the probability that a soft error causes an erroneous output or system state. It can also be used as a guideline for selective hardening of circuit nodes [30].

3 SINGLE EVENT TRANSIENTS - AN UNDERESTIMATED PROBLEM

As soft errors in random logic are a key challenge in nanoscale systems, within the framework of the RealTest Project special emphasis has been placed on modeling the effects of particle strikes in combinational logic [15]. The results of this work have shown that soft errors in random logic are still an underestimated problem. In particular, it has been shown that in the majority of investigated cases soft errors remain in the system about twice as long as predicted by traditional approaches. For a better understanding of these results, the differences between traditional modeling and the refined approach from [15] are pointed out in more detail in the sequel.

A particle strike in combinational logic can cause a glitch in the output voltage of a logic gate [8]. Usually such a "single event transient" (SET) only leads to a system failure, if it can propagate to a register and turn into a single event upset (SEU) there. As a precondition, propagation paths must be sensitized in the logic, and the glitch must arrive at the register during a latch window [23, 31]. In Figure 1 this is illustrated for a small example.
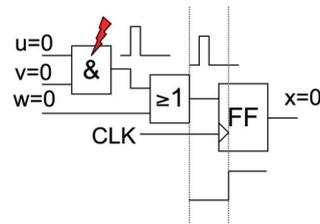
Figure 1: Logical and latch window masking.

If the particle strike at the AND gate produces a glitch at the output, this can only be propagated through the OR gate for $w = 0$. The glitch at the output

of the OR gate is not latched in the FF, because it has disappeared before the next rising edge of the clock. In addition, depending on the amplitude of a glitch, its propagation can also be prevented by electrical masking [9]. Overall, it is particularly important not only to predict the occurrence of an SET but also to accurately characterize its expected shape.

State of the art device simulators allow a precise characterization of SETs, but they are also highly computationally intensive [10]. In many cases circuit level techniques offer a good compromise between accuracy and computational cost [3, 20, 25, 32, 35]. They can also be combined with device level analysis to mixed level approaches [9, 10].

3.1 Refined electrical modeling for particle strikes

Most circuit level approaches model the effect of a particle strike with the help of a transient current source as shown in Figure 2.
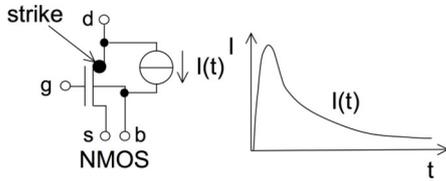
Figure 2: Transient current model.

A common approximation to determine the current slope $I(t)$ is the double exponential function in equation (1) [28]. Here τ_a is the collection time-constant of the pn-junction, and τ_b denotes the time-constant for establishing the electron-hole track.

$$I(t) = I_0 \left(\exp\left(-\frac{t}{\tau_a}\right) - \exp\left(-\frac{t}{\tau_b}\right) \right) \qquad (1)$$

An alternative model is given by formula (2) with parameters Q, τ and K, where Q is the collected charge, τ is a pulse-shaping parameter and K is a constant [11].

$$I(t) = \frac{K \cdot Q}{\tau} \sqrt{\frac{t}{\tau}} \exp\left(-\frac{t}{\tau}\right) \qquad (2)$$

Both models assume a constant voltage V across the pn-junction and do not consider the interdependence between charge collection and the change in voltage over time. This simplification is appropriate for modeling strikes at a significant distance from a pn-junction, where charge is collected by diffusion.

However, if an α-particle or a heavy ion generated by a neutron strike crosses a pn-junction, this leads to a "funneling" process, which has first been described by Hsieh for α-particle strikes [16]. Here, charge collection by drift is the dominating phenomenon, and this process depends on the electric field strength, and thus on the voltage. Among several models for the charge collection by drift, Hu's model has been se-

lected as the basis for the work in [15], because it is also valid for variable field strength [17, 27, 28]. Hu only considers α-particle strikes, but it has been shown by device simulations that ions crossing a pn-junction lead to similar effects [37].

For the sake of simplicity, in the following explanations it is assumed that the particle strikes the pn-junction at an angle of 90°, and the discussion is restricted to NMOS without loss of generality. The particle strike in Figure 3 generates a track of free electron-hole-pairs, which disturbs the depletion zone.
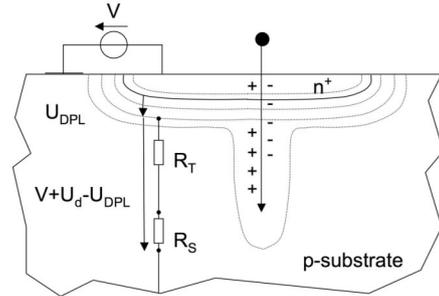
Figure 3: Funneling process.

The electrons from the track are drifting to the drain/source region while the holes are drifting into the substrate generating an electric field. The depletion zone is gradually regenerated in the regions where no holes are left over. This funneling process is finished when all the holes have drifted out of the original depletion zone. To model the current flow Hu assumes an ideal voltage source V as depicted in Figure 3.

In addition to V, the drift current $I_{drift}(t)$ is determined by the diode potential U_d of the pn-junction, the voltage $U_{DPL}(t)$ across the depletion zone, the resistance R_T of the electron-hole-track, and the resistance R_S of the substrate. With $G = (R_T + R_S)^{-1}$ the curve $I_{drift}(t)$ is given by equation (3).

$$I_{drift}(t) = G \cdot \left(V + U_D - U_{DPL}(t) \right) \qquad (3)$$

To determine the voltage $U_{DPL}(t)$ Hu assumes that the charge carrier density is equal to the density N_{sub} of acceptors in the substrate. However, Juhnke has shown by device simulation that this approximation may not be precise enough [19]. Exploiting the condition of quasi-neutrality in semiconductors Juhnke derives an improved model with equation (4) for $U_{DPL}(t)$.

$$U_{DPL}(t) = \frac{K}{N_{eh,l}} \cdot \sqrt{V + U_D} \int_0^t I_{drift}(t') dt' \qquad (4)$$

The parameter $N_{eh,l}$ is the line density of the electron-hole-pairs along the track, which depends on the energy of the particle strike. K is a technology dependent parameter mainly determined by the mobilities of the electrons and holes and by the density of

acceptors in the substrate. Inserting (4) into (3) provides the differential equation (5) for $I_{drift}(t)$.

$$I_{drift}(t) = G \cdot \left(V + U_d - \frac{K}{N_{eh,l}} \cdot \sqrt{V + U_D} \int_0^t I_{drift}(t') dt' \right) \quad (5)$$

For constant voltage V this equation has a closed form solution and Juhnke's model can be summarized by formula (6).

$$I_{drift}(t) = G \cdot (V + U_d) \cdot \exp\left(-\frac{t}{\tau} \right), \quad \tau = \frac{N_{eh,l}}{G \cdot K \sqrt{V + U_D}} \quad (6)$$

As observed in [15] the assumption of constant voltage is only necessary to derive a closed form solution for $I_{drift}(t)$. The term $V + U_d$ in equation (5) can therefore be replaced by a variable voltage $U(t)$, which provides equation (7).

$$I_{drift}(t) = G \cdot \left(U(t) - \frac{K}{N_{eh,l}} \cdot \sqrt{U(t)} \int_0^t I_{drift}(t') dt' \right) \quad (7)$$

With $C(t) = N_{eh,l} / \left(K \cdot \sqrt{U(t)} \right)$ equation (7) can be rewritten to formula (8), which suggests the interpretation as a serial connection of a capacitance and a conductance. Since the capacitance $C(t)$ depends on $U(t)$, the model is also referred to as UGC model.

$$I_{drift}(t) = G \cdot \left(U(t) - \frac{1}{C(t)} \int_0^t I_{drift}(t') dt' \right) \quad (8)$$

State-of-the-art circuit simulators based on advanced description languages such as VHDL-AMS allow the implementation of arbitrary two terminal networks. Thus, it is not necessary to solve equation (7) analytically, but it can be passed directly to the simulator for numerical analysis. A symmetric analysis can be carried out for PMOS devices, but then the network must be connected with opposite polarity and the technology parameter K must be adapted.

First experiments reported in [15] have shown that the traditional transient current model (based on equation (6)) and the UGC model provide significantly different results. Analyzing for example the behavior of a transistor after an α-particle strike of 1 MeV, the glitches in the drain voltage predicted by the UGC model have smaller amplitude but longer duration. To justify this different view on single event transients, the UGC model has been validated by comparing it to the device level analysis of an NMOS transistor reported in [9]. As shown in [15] both the device level simulations and the circuit level simulations using the UGC model yield smaller amplitudes and longer durations than traditional circuit level simulations based on a transient current source.

3.2 Gate level modeling and simulation results

The impact of the UGC model on SEU prediction can be two-fold. On the one hand, smaller amplitudes may increase electrical masking, but on the other hand a longer duration of glitches is likely to increase the probability of propagation through the circuit. In order to analyze the impact of the UGC model in more detail, in [15] the gate level behavior in the presence of SETs has been extracted using standard techniques as described in [1]. The circuit level parameters were based on a 130 nm process, and for each gate full parasitic information was taken into account during extraction. This way a gate library was created and used to synthesize a set of finite state machine benchmarks with the SIS synthesis tool, the characteristics of which are summarized in Table 1 [26, 38].

Table 1. Characteristics of FSM examples

FSM	States	PI	PO	FF	Gates	tc [ps]
bbara	10	4	2	8	90	670
dk14	7	3	5	3	145	993
dk16	27	2	3	5	409	2068
ex5	9	2	2	2	18	348
ex6	8	5	8	3	123	928
fetch	26	9	15	9	210	697
keyb	19	7	2	8	333	905
lion	4	2	1	2	20	308
mc	4	3	5	9	50	381
nucpwr	29	13	27	5	271	568
s1	20	8	6	8	199	1159
sand	32	11	9	21	928	1186
scf	122	27	56	24	1280	1668
shiftreg	8	1	1	4	16	209
styr	30	9	10	5	767	2677
sync	52	19	7	33	529	1403
train11	11	2	1	2	15	211

The columns show the names of the finite state machines, the number of states, the number of primary inputs and outputs, the number of flip-flops and the number of gates after state minimization, state coding and logic minimization as well as the minimum cycle times in picoseconds.

For the simulation at the gate level with a state of the art event driven simulator, the properties of the library cells were mapped to VHDL behavioral descriptions. To model electrical masking at the gate level, the observations reported in [7] were exploited. Electrical masking is most pronounced in the first two logic levels after the struck node and after this, electrical masking effects can be neglected and strictly Boolean behavior can be assumed.

To quantify the impact of the UGC model, the following simulation flow is reported in [15]. The behavior of a finite state machine is monitored during a given number of cycles with a random input sequence. To compare the UGC model to the common model based on a transient current source, in fact three copies of the finite state machine are simulated under

exactly the same conditions. In each clock cycle a random SET is injected into the combinational logic of the finite state machine: an SET characterized by the UGC model in one copy and an SET characterized by a transient current source into the other copy. For comparison the third copy simulates the fault free case. If the SET cannot propagate to a flip-flop in neither copy, then the next SET is injected in the next cycle. Otherwise, a checkpoint for the simulation of the good machine is generated, and the simulation is continued until a fault free state is reached again. This way it can be determined how long the fault effects remain in the system, which can be used as a measure of the "severity" of the faults [12]. If the fault effects remain in the system for more than a given limit, then the analysis is stopped to save simulation time. After the states of both copies agree with the good machine or the analysis of fault effects has been stopped, the checkpoint for the simulation of the good machine is restored, and simulation continues with the injection of the next SET.

For the first series of experiments in [15], a clock of maximum frequency was assumed while monitoring the finite state machine for 10 million SET injections. The results showed that once an SET manifested itself as an SEU in the system, the average time for the SEU to stay in the system was similar for both the UGC and the traditional transient current model. However, comparing the number of occurrences of SEUs showed significantly different results for both models. To simplify the discussion of the results in the following let t_{UGC} denote the number of cycles an SET remains in the system when the simulation is based on the UGC model, and let t_{trans} represent the same number for the transient current model. Furthermore, the number of SETs with $t_{UGC} > k$ is denoted by $n(t_{UGC} > k)$, and the number of SETs with $t_{trans} > k$ is denoted by $n(t_{trans} > k)$.

In particular, a value of t_{UGC} or t_{trans} larger than zero means that the SET has been propagated to one or more registers, consequently causing an SEU. In sequential circuits an SEU can sometimes be tolerated, if it remains in the system only for or a few clock cycles and the system recovers quickly to fault free operation [12]. But if it repeatedly propagates through the next state logic and stays in the system for many cycles, then the risk of a severe system failure increases considerably. Thus, it is also particularly important to compare the results for the number of SEUs staying in the system for more than a tolerable number of cycles.

Figure 4 compares $n(t_{UGC} > 0)$ and $n(t_{trans} > 0)$ as well as $n(t_{UGC} > 20)$ and $n(t_{trans} > 20)$. For each circuit, the left bar shows the ratio $n(t_{UGC} > 0)/n(t_{trans} > 0)$, and the right bar represents the ratio $n(t_{UGC} > 20)/n(t_{trans} > 20)$. There are some cases where no SEUs stayed in the system for more than 20 cycles in both cases. Here the respective bars are omitted.
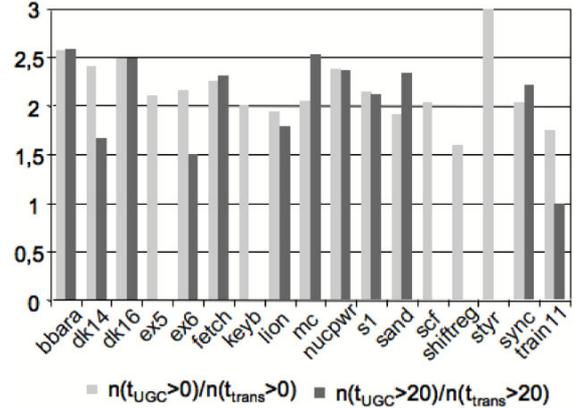
Figure 4: Comparing the ratios $n(t_{UGC} > 0)/n(t_{trans} > 0)$, and $n(t_{UGC} > 20)/n(t_{trans} > 20)$ for maximum frequency.

It can be observed that the major trend is a factor of two between the UGC model and the transient current source model. This implies that the more realistic prediction by the UGC model results in twice as many (severe) SEUs as a prediction by the traditional transient current model.

The detailed results in [15] show that there are also some cases where the transient current source model predicts longer times for the SEUs to stay in the system. In this case the smaller amplitudes predicted by the UGC model result in electrical masking. But five to ten times more often the longer duration of glitches is the dominating effect.

Although the probability for an SET to be latched in a flip-flop increases with the operating frequency, these trends have been confirmed also for simulations based on different clock frequencies [15].

4 CONCLUSIONS

The increasing variability of parameters and the increasing vulnerability to defects, degradation, and transient faults require a paradigm shift in design and test of nanoscale systems. A robust and fault tolerant system design becomes mandatory also for non critical applications, and testing has to characterize not only the functionality but also the robustness of a system.

The RealTest Project addresses these problems by developing unified design and test strategies supporting both a robust design and efficient test procedures for manufacturing test as well as online test and fault tolerance.

First results concerning the susceptibility of random logic to soft errors have shown that the effects of SETs have still been underestimated so far. Simulations at gate level based on a refined electrical model for SETs have revealed about twice as many critical effects as simulations based on a traditional model.

6

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