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A Refined Electrical Model for Particle Strikes and its Impact on SEU Prediction

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Abstract

Decreasing feature sizes have led to an increased vulnerability of random logic to soft errors. A particle strike may cause a glitch or single event transient (SET) at the output of a gate, which in turn can propagate to a register and cause a single event upset (SEU) there.

Circuit level modeling and analysis of SETs provides an attractive compromise between computationally expensive simulations at device level and less accurate techniques at higher levels. At the circuit level particle strikes crossing a pn-junction are traditionally modeled with the help of a transient current source. However, the common models assume a constant voltage across the pn-junction, which may lead to inaccurate predictions concerning the shape of expected glitches. To overcome this problem, a refined circuit level model for strikes through pn-junctions is investigated and validated in this paper. The refined model yields significantly different results than common models. This has a considerable impact on SEU prediction, which is confirmed by extensive simulations at gate level. In most cases, the refined, more realistic, model reveals an almost doubled risk of a system failure after an SET.

1. Introduction

Nowadays, a saturation of the soft error rate (SER) in memories can be observed, while technology scaling has led to an increased vulnerability of combinational logic and latches. Soft error mitigation for random logic has become a topic of major importance [1, 13, 23, 26]. Here, a wide spectrum of strategies is possible, such as voltage scaling, robust flip-flop design, selective hardening or self-checking circuit design. However, in order to choose the best approach for a certain application and to determine the necessary degree of protection, effective techniques are needed for characterizing a circuit's sensitivity to soft errors as accurately as possible.

A particle strike in combinational logic can cause a glitch in the output voltage of a logic gate. Usually such a "single event transient" (SET) only leads to a system failure, if it can propagate to a register and turn into an SEU there. As a precondition, propagation paths must be sensitized in the logic, and the glitch must arrive at the register during a latch window [18, 24]. But, depending on the amplitude and the duration of a glitch, its propagation can also be prevented by electrical masking [8]. Thus, it is particularly important not only to predict the occurrence of an SET but also to accurately characterize its expected shape.

State of the art device simulators allow a precise characterization of SETs, but they are also highly computationally intensive [9]. In many cases circuit level techniques offer a good compromise between accuracy and computational cost [2, 17, 19, 25]. Mixed-level approaches combine device level analysis for a few devices with circuit level analysis for the rest of the circuit [8, 9].

At circuit level, common models for SETs work with a transient current source based on analytical models as for example described in [11] or [22]. As it will be explained in Section 2, this well reflects charge collection by diffusion, but it may lead to less accurate predictions for particle strikes crossing a *pn*-junction, where charge is mainly collected by drift. The problem is that the varying voltage across the *pn*-junction is not taken into account in this case [16, 28].

To overcome this problem, this paper investigates a refined circuit level model for the charge collection by drift, which allows a variable voltage across the *pn*-junction. It will be shown that the refined model closely matches the results reported in [8], which have been obtained by device simulation. The behavior predicted by the refined model is significantly different from the traditional models. Namely, glitches have smaller amplitudes but longer durations, and consequently higher SEU rates than previously assumed must be associated with SETs. To quantify the impact of the refined model on the SEU prediction, a gate library has been characterized using both the refined and the traditional model, and gate level simulations for a set of finite state machine benchmarks have been performed.

2. Circuit level SET models - state of the art

Particle strikes in logic circuits can roughly be divided into two categories [7]. In the first case, an ion generates an electron-hole-track in the substrate at a significant distance from a *pn*-junction, and the charge carriers are transported mainly by diffusion. In the second case, an α-particle or a heavy ion generated by a neutron strike crosses a *pn*-junction. This leads to a "funneling" process, which has first been described by Hsieh for α-particle strikes [14]. Here, charge collection by drift is the dominating phenomenon.

As models based on critical charge cannot provide information about the amplitude and duration of a single event transient, they are not considered in this work [11]. Most other circuit level approaches model the effect of a particle strike with the help of a transient current source as shown in Figure 1.

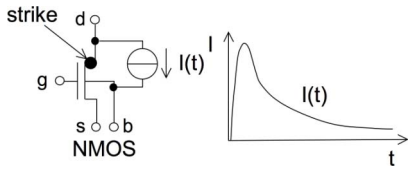

Figure 1: Particle strike modeled by a transient current source.

A common approximation to determine the current slope $I(t)$ is the double exponential function in equation (1a) [22]. Here τ_a is the collection time-constant of the *pn*-junction, and τ_b denotes the time-constant for establishing the electron-hole track. An alternative model is given by formula (1b) with parameters Q, τ and K, where Q is the collected charge, τ is a pulse-shaping parameter and K is a constant [11].

$$(a) \quad I(t) = I_0\left(\exp\left(-\frac{t}{\tau_a}\right) - \exp\left(-\frac{t}{\tau_b}\right)\right) \qquad (b) \quad I(t) = \frac{K \cdot Q}{\tau}\sqrt{\frac{t}{\tau}}\exp\left(-\frac{t}{\tau}\right) \tag{1}$$

Both models assume a constant voltage V across the *pn*-junction and do not consider the interdependence between charge collection and the change in voltage over time. This simplification is appropriate for modeling diffusion, but charge collection by drift depends on the electric field strength, and thus on the voltage. Therefore, in [5] an extended model is proposed. However, this model still neglects the fact that the duration of the current flow also depends on the voltage. Consequently, the duration of glitches at the outputs of logic gates cannot be characterized precisely.

To analyze strikes close to a *pn*-junction, models for the charge collection by drift must be reviewed in more detail [15, 21, 22]. As Hu's model is also valid for variable field strength, it is described in the sequel [15]. Hu only considers α-particle strikes, but it has been shown by device simulations that ions crossing a *pn*-junction lead to similar effects [27]. The analysis is carried out for an α-particle which strikes a *pn*-junction at an angle θ and crosses the depletion zone. For the sake of simplicity, in the following explanations θ is assumed to be 90° and the discussion is restricted to NMOS without loss of generality. The particle strike in Figure 2 generates a track of electron-hole-pairs, which disturbs the depletion zone. The electrons from the track are drifting to the drain/source region while the holes are drifting into the substrate. The depletion zone is gradually regenerated in the regions where no holes are left over. This funneling process is finished when all the holes have drifted out of the original depletion zone. To model the current flow Hu assumes an ideal voltage source V as depicted in Figure 2.

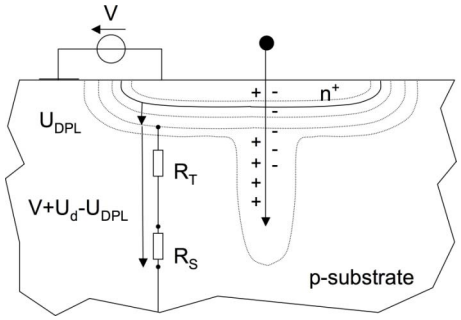

Figure 2: Intermediate phase of the funneling process.

In addition to V, the drift current $I_{drift}(t)$ is determined by the diode potential U_d of the *pn*-junction, the voltage $U_{DPL}(t)$ across the depletion zone, the resistance R_T of the electron-hole-track, and the resistance R_S of the substrate. With $G = (R_T + R_S)^{-1}$ the curve $I_{drift}(t)$ is given by equation (2).

$$I_{drift}(t) = G \cdot \left(V + U_d - U_{DPL}(t)\right) \tag{2}$$

To determine the voltage $U_{DPL}(t)$ Hu assumes that the charge carrier density is equal to the density N_{sub} of acceptors in the substrate. However, Juhnke has shown by device simulation that this approximation may not be precise enough [16]. To derive an improved model, Juhnke exploits the condition of quasi-neutrality in semiconductors. The *p*-side of the depletion zone must contain additional electrons to reach the same charge Q_{n+} as the *n*+-side of the depletion zone. This results in equations (3a) and (3b) for $U_{DPL}(t)$.

$$(a) \quad U_{DPL}(t) = \frac{Q_{n^+}}{2\varepsilon_{Si}} \cdot \frac{\mu_p}{\mu_n + \mu_p} \cdot \frac{1}{qN_{eh,l}} \int_0^t I_{drift}(t')dt' \qquad (b) \quad Q_{n^+} = \sqrt{2\varepsilon_{Si} q N_{sub} \left(V + U_d\right)} \tag{3}$$

The parameter $N_{eh,l}$ is the line density of the electron-hole-pairs along the track, q denotes the charge of an electron, μ_n and μ_p characterize the mobilities of electrons and holes, and ε_{Si} is the di-electric constant of silicon. Inserting (3a) into (2) provides the differential equation (4) for $I_{drift}(t)$. For constant voltage V this equation has a closed form solution as detailed in formulas (5a) and (5b).

$$I_{drift}(t) = G \cdot \left(V + U_d - \frac{Q_{n^+}}{2\varepsilon_{Si}} \cdot \frac{\mu_p}{\mu_n + \mu_p} \cdot \frac{1}{qN_{eh,l}} \int_0^t I_{drift}(t')dt' \right) \tag{4}$$

$$(a) \quad I_{drift}(t) = G \cdot \left(V + U_d\right) \cdot \exp\left(-\frac{t}{\tau}\right) \qquad (b) \quad \tau = \frac{2\varepsilon_{Si} q N_{eh,l}}{Q_{n^+} G} \left(1 + \frac{\mu_n}{\mu_p}\right) \tag{5}$$

3. Refined circuit level modeling

As explained above, the assumption of constant voltage can lead to inaccuracies in analyzing charge collection by drift. However, the review of both Hu's and Juhnke's approach in Section 2 shows that this assumption is only necessary to derive a closed form solution for $I_{drift}(t)$ [15, 16]. Therefore the term $V + U_d$ in equations (3) and (4) can be replaced by a variable voltage $U(t)$, which provides equation (6).

$$I_{drift}(t) = G \cdot \left(U(t) - \frac{\sqrt{qN_{sub}U(t)}}{\sqrt{2\varepsilon_{Si}}} \cdot \frac{\mu_p}{\mu_n + \mu_p} \cdot \frac{1}{qN_{eh,l}} \int_0^t I_{drift}(t')dt' \right) \tag{6}$$

Accumulating the technology dependent constants into one parameter K, the simplified representation by formula (7) is obtained. The line density $N_{eh,l}$ of the electron-hole-pairs along the track depends on the energy of the particle and is shown as an extra parameter.

$$I_{drift}(t) = G \cdot \left(U(t) - \frac{K}{N_{eh,l}} \cdot \sqrt{U(t)} \int_0^t I_{drift}(t')dt' \right) \tag{7}$$

With $C(t) = N_{eh,l} \Big/ \left(K \cdot \sqrt{U(t)} \right)$ equation (7) can be rewritten to formula (8), which suggests the interpretation as a serial connection of a capacitance and a conductance. Since the capacitance $C(t)$ depends on $U(t)$, the model is also referred to as UGC model.

$$I_{drift}(t) = G \cdot \left(U(t) - \frac{1}{C(t)} \int_0^t I_{drift}(t')dt' \right) \tag{8}$$

State-of-the-art circuit simulators based on advanced description languages such as VHDL-AMS allow the implementation of arbitrary two terminal networks (cf. IEEE Std. 1076.1). Thus, it is not necessary to solve equation (6) analytically, but it can be passed directly to the simulator for numerical analysis. A symmetric analysis can be carried out for PMOS devices, but then the two terminal network must be connected with opposite polarity and the technology parameter K in (7) must be adapted. The refined model has been integrated into Qimonda's circuit simulator Titan [10]. Comparing it to the transient current model based on equation (5) shows a significant difference between both models. Analyzing for example the behavior of a transistor after an α-particle strike, the glitches in the drain voltage predicted by the refined model have smaller amplitude but longer duration. Smaller amplitudes may lead to electrical masking, but on the other hand the longer duration of glitches may dominate this effect and increase the probability of propagation through the circuit. To justify this more pessimistic view on single event transients, the new model has been validated by comparing the device level analysis of a transistor reported in [8] to circuit level simulation with the refined model.

The experiment in [8] analyzes the propagation of ion strikes in a chain of 10 inverters using a commercial device and circuit level simulator. The strikes in the NMOS transistor of the first inverter are described by a 3D device model, while the rest of the circuit is simulated at circuit level. The results from [8] for the NMOS transistor are reproduced in Figure 3. As shown by earlier experiments validating the accurateness of 3D device simulations, these results can be considered as very realistic [6]. The simulated drain voltage transients are shown for several particle strikes characterized by the linear energy transfer (LET), i.e. the energy loss per unit path length when the particles pass through the material. From the LET value, the line density $N_{eh,l}$ of electron-hole-pairs along the track can be computed.

The experiment in [8] has been repeated using circuit simulation only. Figure 4a shows that relying on a transient current source based on equation (5) cannot appropriately reflect the trends revealed by device simulation. The curves for device simulation show a longer duration of glitches and smaller amplitudes than the respective curves for the transient current model.

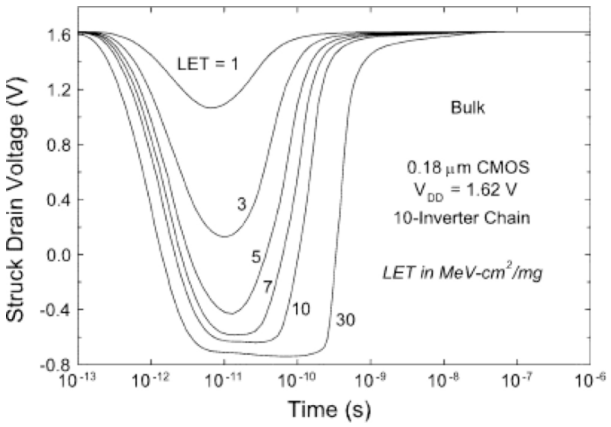

Figure 3: Device level analysis of an NMOS transistor [8].

It is important to note that an exact matching of results cannot be expected, because not all the parameters used in [8] were available. Nevertheless, as illustrated in Figure 4b, the results achieved with the improved simulator clearly show the same trends as the curves from [8].

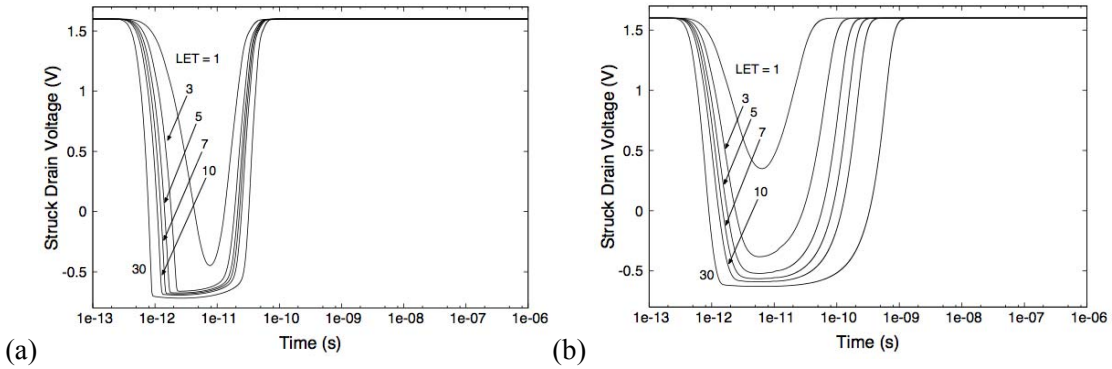

Figure 4: Circuit simulation using a transient current (a) and the UGC model (b).

Both the device level simulations and the circuit level simulations using the UGC model yield smaller amplitudes and longer durations than traditional circuit level simulations based on a transient current source.

4. Gate level modeling

In order to analyze the impact of the UGC model on SEU prediction for logic circuits, the gate level behavior in the presence of SETs has been extracted using standard techniques. The circuit level parameters were based on a 130 nm process, and for each gate full parasitic information was taken into account during extraction. This way a gate library of NAND and NOR gates as well as inverters was created. In particular, the gate delay was determined for each gate with 3 different capacitive loads. Furthermore, every gate was characterized using exhaustive electrical fault simulation, for all possible gate input assignments and all fault injections possible in the layout.

For the simulation at the gate level with a state of the art event driven simulator, the properties of the library cells have been mapped to VHDL behavioral descriptions. To model electrical masking at the gate level, the observations reported in [3] have been exploited. Electrical masking is most pronounced in the first two logic levels after the struck node and

after this, electrical masking effects can be neglected and strictly Boolean behavior can be assumed. Therefore electrical masking can be characterized by a parameter showing how many logic levels have been passed. Overall, a signal at the gate level is described by a tuple listing the logic value, the number of logic levels since fault injection, the inverter equivalent fanout loads through which the fault has passed, and the fault injection mechanism such as charge and the transistor node that has been struck. The tuple points to a table with pre-calculated values for the SET widths depending on the parameters attached to the signal.

As it was not the purpose of this work to improve the simulation techniques for SETs at the gate level, a commercial simulator was used for a prototype implementation. To speed up simulation time, more advanced techniques can of course be applied with the derived models [4].

5. Simulation results

The gate library described in Section 4 has been used to synthesize a set of finite state machine benchmarks with the SIS synthesis tool [20, 29]. The circuit characteristics are shown in Table 1. The columns list the names of the finite state machines, the number of states, the number of primary inputs and outputs, the number of flip-flops and the number of gates after state minimization, state coding and logic minimization as well as the minimum cycle times in picoseconds.

Table 1. Characteristics of FSM examples.

FSM	States	PI	PO	FF	Gates	tc [ps]
bbara	10	4	2	8	90	670
dk14	7	3	5	3	145	993
dk16	27	2	3	5	409	2068
ex5	9	2	2	2	18	348
ex6	8	5	8	3	123	928
fetch	26	9	15	9	210	697
keyb	19	7	2	8	333	905
lion	4	2	1	2	20	308
mc	4	3	5	9	50	381

FSM	States	PI	PO	FF	Gates	tc [ps]
nucpwr	29	13	27	5	271	568
s1	20	8	6	8	199	1159
sand	32	11	9	21	928	1186
scf	122	27	56	24	1280	1668
shiftreg	8	1	1	4	16	209
styr	30	9	10	5	767	2677
sync	52	19	7	33	529	1403
train11	11	2	1	2	15	211

To quantify the impact of the UGC model, the following simulation flow has been implemented. The behavior of a finite state machine is monitored during a given number of cycles with a random input sequence. To compare the UGC model to the common model based on equation (5), in fact three copies of the finite state machine are simulated under exactly the same conditions. In each clock cycle a random SET is injected into the combinational logic: an SET characterized by the UGC model in one copy and an SET characterized by the transient current model into the other copy. For comparison the third copy simulates the fault free case. If the SET cannot propagate to a flip-flop in neither copy, then the next SET is injected in the next cycle. Otherwise, a checkpoint for the simulation of the good machine is generated, and the simulation is continued until a fault free state is reached again. This way it can be determined how long the fault effects remain in the system, which can be used as a measure of the "severity" of the faults [12]. If the fault effects remain in the system for more than a given limit, then the analysis is stopped to save simulation time. After the states of both copies agree with the good machine or the analysis of fault effects has been stopped, the checkpoint for the simulation of the good machine is restored, and simulation continues with the injection of the next SET.

A first series of simulations has been performed assuming a clock of maximum frequency for each circuit while monitoring the finite state machine for 10 million SET injections. The results are shown in Table 2. In all columns t_{UGC} denotes the number of cycles an SET remains in the system when the simulation is based on the UGC model, and t_{trans} represents the same number for the transient current model. To simplify the discussion of the results in the following, the number of SETs with $t_{UGC} > k$ is denoted by $n(t_{UGC} > k)$, and the number of SETs with $t_{trans} > k$ is denoted by $n(t_{trans} > k)$.

Comparing the average numbers $t_{avg,UCG}$ and $t_{avg,trans}$ in the second and third column shows quite a similar behavior for both models. However, the average numbers have been derived on the basis of actually occurred SEUs for each model, not on the basis of all SET injections. Therefore, it is more interesting to compare the number of occurrences of SEUs shown in the remaining columns. A value of t_{UGC} or t_{trans} larger than zero means that the SET has been propagated to one or more registers causing an SEU. The results in Table 2 show that the observations in Section 3 directly translate to the behavior in sequential circuits. Comparing $n(t_{UGC} > 0)$ and $n(t_{trans} > 0)$ reveals that SETs according to the UGC model cause almost twice as many SEUs than SETs according to the traditional model.

Table 2. Results for maximum frequency and 10 million injected SETs.

FSM	$t_{avg,UGC}$	$t_{avg,trans}$	Number of SETs with					
			$t_{UGC} > 0$	$t_{UGC} > 20$	$t_{trans} > 0$	$t_{trans} > 20$	$t_{UGC} > t_{trans}$	$t_{trans} > t_{UGC}$
bbara	6.2	6.0	101,696	4,205	39,643	1,626	70,026	6,684
dk14	2.9	3.0	59,507	5	24,788	3	42,144	8,714
dk16	7.0	6.9	28,429	1,172	11,454	471	20,535	3,444
ex5	1.2	1.1	253,257	0	120,257	0	164,210	22,032
ex6	2.4	2.4	60,356	3	27,895	2	41,269	8,394
fetch	21.5	21.0	152,943	67,439	68,042	29,271	103,833	17,157
keyb	1.8	1.8	52,475	0	26,098	0	34,791	6,826
lion	5.0	5.2	379,638	5,435	195,632	3,031	243,732	68,319
mc	5.0	4.2	177,611	6,670	86,737	2,635	115,493	17,838
nucpwr	37.9	38.1	144,675	108,778	60,849	45,989	99,853	15,762
s1	4.3	4.3	84,556	533	39,381	252	56,956	11,852
sand	29.3	24.3	43,077	25,987	22,465	11,163	27,378	5,826
scf	2.3	2.3	49,237	0	24,272	0	31,266	5,607
shiftreg	1.9	1.7	476,467	0	297,671	0	270,710	33,238
styr	1.8	1.7	15,629	0	5,221	0	11,782	1,322
sync	28.1	25.9	100,048	55,043	49,224	24,913	64,160	10,991
train11	2.2	2.0	412,076	1	235,661	1	251,008	52,785

In sequential circuits an SEU can sometimes be tolerated, if it remains in the system only for a few clock cycles [12]. But if it repeatedly propagates through the next state logic and stays in the system for many cycles, then the risk of a severe system failure increases considerably. Therefore, it is important to compare also the results for the number of SEUs staying in the system for more than a tolerable number of cycles (20 cycles in our experiments). As Figure 5 indicates, here the same quantitative trends can be observed as for $n(t_{UGC} > 0)$ and $n(t_{trans} > 0)$. For each circuit, the left bar shows the ratio $n(t_{UGC} > 0)/n(t_{trans} > 0)$, and the right bar represents the ratio $n(t_{UGC} > 20)/n(t_{trans} > 20)$. There are some cases where no SEUs stayed in the system for more than 20 cycles in both cases. Here the respective bars are omitted. It can be observed

that the major trend is a factor of two between the UGC model and the transient current source model. However, the factors in Figure 5 are derived from the accumulated results and do not show a comparison for individual faults. There are also some cases where the transient current source model leads to more pessimistic results than the UGC model, which is shown by the numbers for $t_{trans} > t_{UGC}$ in Table 2. Here, the smaller amplitudes of the glitches predicted by the UCG model are dominating and lead to an increased electrical masking. But the respective numbers for $t_{UGC} > t_{trans}$ are between five to ten times higher. This confirms the conjecture in Section 3 that the longer duration of the glitches is the dominating effect in most cases.

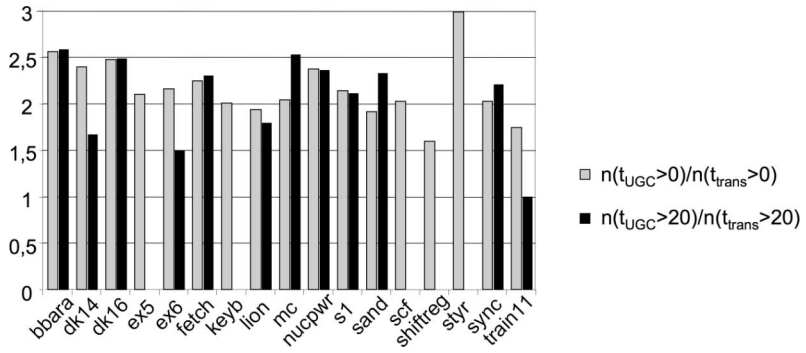

Figure 5: Comparing t_{UGC} and t_{trans} for maximum frequency.

Furthermore, the results in Table 2 also show a varying susceptibility to SEUs of the circuits under investigation. Clearly, the probability for an SET to be latched in a flip-flop increases with the operating frequency. For example, *shiftreg* and *train* are the circuits with the lowest cycle time and exhibit the highest SEU rate of all the simulated circuits. On the other hand, an SEU in these circuits is less likely to remain in the system for more than a few cycles. To analyze whether the differences between the UGC model and the transient current source model also depend on the frequency, the simulations have been repeated at reduced clock rates. As expected, due to the reduced latching probability at lower frequency less SEUs have been observed for the same number of SETs. However, analyzing the same parameters and relations as before yields similar trends again. The only exceptions are circuits *ex6*, *train11,* and *shiftreg*. For *ex6* both $n(t_{UGC} > 20)$ and $n(t_{trans} > 20)$ have become zero, and for *train11* and *shiftreg* the difference between the UGC and the transient current model with respect to the time an SEU is predicted to stay in the system is increased even further.

6. Conclusions

Circuit level modeling of SETs plays an important role for SEU prediction also at higher levels. Traditionally transient current sources have been used to characterize SETs. For SETs caused by particle strikes close to *pn*-junctions, where charge collection by drift is the major effect, the underlying assumption of constant voltage may lead to inaccurate predictions concerning the amplitude and duration of SETs. In this paper a refined model has been proposed which allows a variable voltage across the *pn*-junction.

Simulation results at gate level have shown that modeling SETs with the refined model in most cases reveals about twice as many critical effects as relying on a traditional model. Single event transients must thus be considered as more harmful than assumed before. The proposed refined model can help to identify risks for system failures more accurately and better guide through available strategies for soft error mitigation.

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