Poster Summaries

A Synthesis Approach to Reduce Scan Design Overhead

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Today's logic design strategy is characterized by a division between synthesis, in which a functionally correct implementation is generated, and design for testability, in which the implementation is made testable. We propose to merge these two steps by utilizing a scan path structure to simplify the combinational logic of finite state machines (FSM's).

Using a Johnson counter instead of D-type flipflops as state memory can reduce the amount of combinational logic to implement as FSM [AmEB 88]. With only minor modifications, a scan path through the FSM flipflops can be converted to a Johnson counter. By utilizing the functionality of the scan chain in system mode, the PLA area for implementing the combinational logic of typical industrial controllers can be reduced by about 10%. With a proper implementation of the Johnson counter, the testability of the resulting structure is not impaired.

This results in a reduction of test overhead, because a part of the scan path is already incorporated during the synthesis process. Alternatively, it can be seen as using a new optimization potential in logic synthesis, since the circuit has to be made testable anyway and so the test hardware is provided "free".

[AmED 88] R Amann, B Eschermann, U Baitinger: PLA Based Finite State Machines Using Johnson Counters as State Memories; Proc. IEEE International Conference on Computer Design, pp. 267-270, 1988.