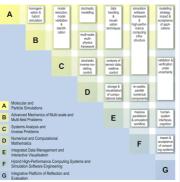
# Mapping Simulation Algorithms to Parallel Architectures



## The Challenge

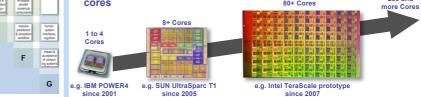
SimTech

- Modern simulation algorithms demand enormous amounts of computing power
- SimTech Research Areas A F:
   E.g. Molecular and Particle
   Simulation, etc.
- Problem: Very long turn around times limit the usage of simulation



## The Technology

The steady increase of clock frequency has reached its limits
 Nonetheless: Much more computing power is still needed
 Architectures move from classic Single-Core to Multi-Core
 The future will bring Many-Core architectures with thousands of
 Cores



## A First Case Study: Simulation of Quantum Mechanics in Parallel

Cooperation with Prof. Dr. H.-J. Werner, Institute for Theoretical Chemistry

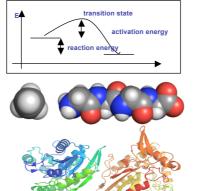
#### Calculating total energies ab initio

#### Important for:

- Reaction energies
- Determining transition states
- Chemical analysis, material research

## Today: Calculations of molecules up to 100 atoms

- Future:
- Investigation of complex biological systems
   Calculations of molecules up to thousands of atoms

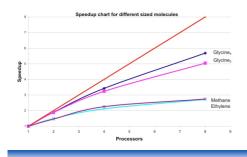


- Interdisciplinary work with student participation
- MOLPRO: (Commercial) program for molecular
- electronic structure calculations
- Calculations of integrals and large matrices
- Coarse-grain parallelization on a 8 core system

	Methane (CH <sub>4</sub> )	
Matrix dimensions	140x140	1100x1100
Disk space needed	80 MB	330 GB
Elapsed time on single cpu	< 1min	40 h

### The Next Steps & Future Work

- On a system with 8 cores a speedup of nearly 6 could be reached
- Next Step: Parallelization for Many-Core architectures with thousands of cores



Abteilung Rechnerarchitektur Prof. Dr. rer. nat. H.-J. Wunderlich Graphics Processing Units (GPU):

•GPUs offer 240+ cores and can be linked

to Multi-GPU systems

•GPGPU: Research on general-purpose calculations on GPUs



#### **Outlook:**

•Effective mapping of simulation problems to thousands of cores

Coarse and fine grain parallelization
Research on other par. architectures
How can reconfigurable HW be used to
support and simplify the mapping?
Thousands of cores: How can fault
tolerance (HW & SW) be guaranteed to
ensure maximum performance and
maximum availability?



### Kontakt:

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