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Cluster of Excellence in Simulation Technology

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Project
PN 2-8

Fast and Accurate Characterization of Approximate Computing Designs on Heterogeneous Computer Architectures

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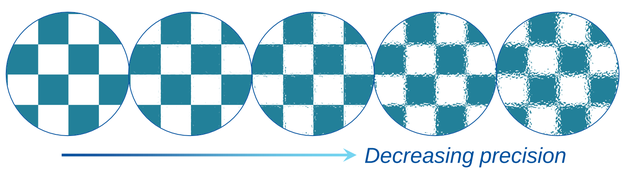
Motivation

Approximate Computing

- Trade-off precision for power, energy, computational performance, and chip area
- Often limited to applications with inherent error tolerance



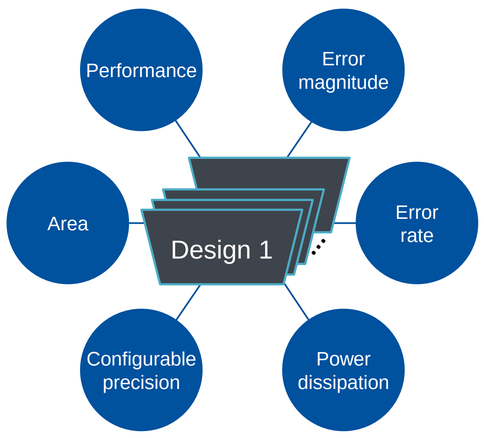
Approximate Computing in image processing

Applying Approximate Computing to Simulation Technology

- Tight accuracy constraints
- Often low error resilience

Approximate Computing Design Space

- Approximate arithmetic units and memories
- Parameters allow to adapt approximation



Design space exploration

Goal: Find suitable design options and parameters

- Increase energy efficiency and ensure acceptable results for scientific applications

Challenges:

- Approximate computing designs constitute a large design space
- Scientific applications comprise billions of instructions
- Evaluation of every instruction not feasible – long runtimes

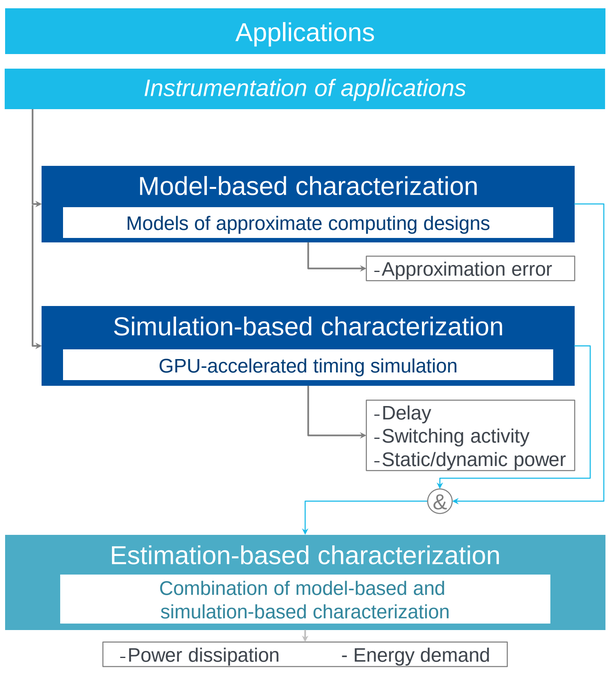
Method

Characterization of Design Options

- Determine performance, power dissipation, and error in application outputs
- Requires compute-intensive hardware simulation

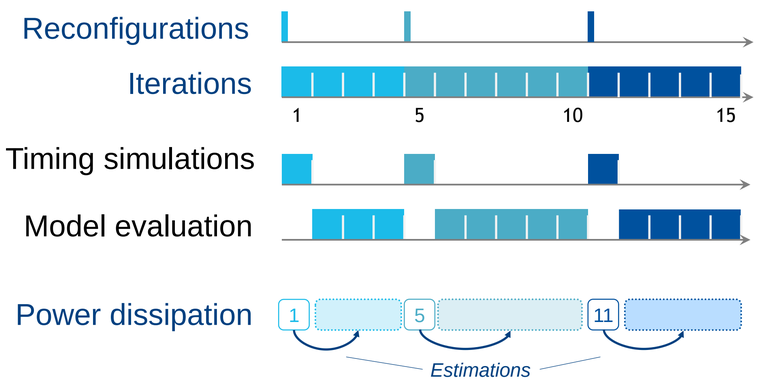
Reduction of characterization runtime

- Identify and exploit iterative methods
- Combination of compute-intensive hardware simulation and light-weight software-based models
- Heterogeneous computer architectures to accelerate hardware simulation[1]



Estimation of power dissipation for an iterative method

- Perform timing simulation to evaluate one iteration after reconfiguration of precision



Experimental Results

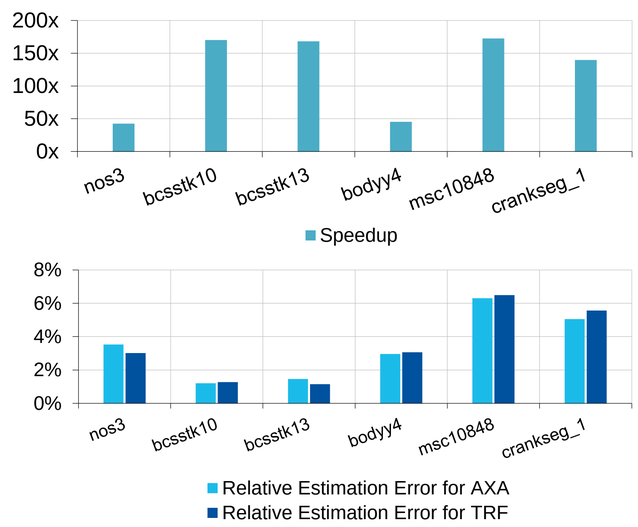
Preconditioned Conjugate Gradient (PCG) on approximate hardware with guaranteed result accuracy

- Important sparse linear system solver
- Efficient fault tolerance methods to monitor and adapt approximation at runtime

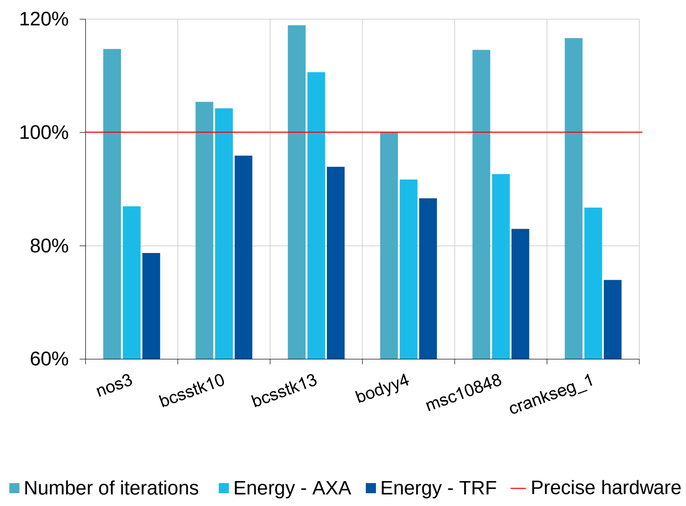
Comparison of two approximate design options against precise hardware

- TRF – Truncation and random fill
- AXA – Approximate adders

Comparison of simulation-based and estimation-based characterization



Energy and iteration count of PCG compared to execution on precise hardware



[1] S. Holst, M. E. Imhof, and H.-J. Wunderlich, "High-Throughput Logic Timing Simulation on GPGPUs", ACM Transactions on Design Automation of Electronic Systems (TODAES), vol. 20, no. 3, pp. 1-22, 2015.
[2] A. Schöll, C. Braun, and H.-J. Wunderlich, "Applying Efficient Fault Tolerance to Enable the Preconditioned Conjugate Gradient Solver on Approximate Computing Hardware", in Proceedings of the 29th Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, DFT'16, University of Connecticut, USA, 19. – 20. September, 2016 , pp. 21 - 26. DFTS Best Paper Award 2016.
[3] A. Schöll, C. Braun, and H.-J. Wunderlich, "Energy-efficient and Error-resilient Iterative Solvers for Approximate Computing", in Proceedings of the 23rd IEEE International Symposium on On-Line Testing and Robust System Design, IOLTS'17, Thessaloniki, Greece, July 3-5, 2017.
[4] A. Schöll, C. Braun, M. A. Kochte, and H.-J. Wunderlich, "Low-Overhead Fault-Tolerance for the Preconditioned Conjugate Gradient Solver", in Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, DFT'15, Amherst, MA, USA, 12.-14. October, 2015, pp. 60-66.