Fast and Accurate Characterization of Approximate Computing Designs on Heterogeneous Computer Architectures

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Motivation

Approximate Computing
- Trade-off precision for power, energy, computational performance, and chip area
- Often limited to applications with inherent error tolerance

Approximate Computing Design Space
- Approximate arithmetic units and memories
- Parameters allow to adapt approximation

Goal: Find suitable design options and parameters
- Increase energy efficiency and ensure acceptable results for scientific applications

Challenges:
- Approximate computing designs constitute a large design space
- Scientific applications comprise billions of instructions
- Evaluation of every instruction not feasible – long runtimes

Method

Characterization of Design Options
- Determine performance, power dissipation, and error in application outputs
- Requires compute-intensive hardware simulation

Reduction of characterization runtime
- Identify and exploit iterative methods
- Combination of compute-intensive hardware simulation and light-weight software-based models
- Heterogeneous computer architectures to accelerate hardware simulation

Estimation of power dissipation for an iterative method
- Perform timing simulation to evaluate one iteration after reconfiguration of precision

Experimental Results

Preconditioned Conjugate Gradient (PCG) on approximate hardware with guaranteed result accuracy
- Important sparse linear system solver
- Efficient fault tolerance methods to monitor and adapt approximation at runtime

Comparison of two approximate design options against precise hardware
- TRF – Truncation and random fill
- AXA – Approximate adders

Energy and iteration count of PCG compared to execution on precise hardware