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Institut für Technische Informatik - Abteilung Rechnerarchitektur
Universität Stuttgart

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Vorwort

Test und Fehlertoleranz sowie Sicherheit und Zuverlässigkeit sind wesentliche Voraussetzungen für den Einsatz informationstechnischer Systeme. Wirtschaftlich bedeutende Bereiche wie die Automobiltechnik oder Industrie 4.0 können nur entwickelt werden, wenn die Verlässlichkeit der zugrundeliegenden Systeme quantifiziert und garantiert werden kann.

Auch im Jahr 2014 konnte der Lehrstuhl Rechnerarchitektur des Instituts für Technische Informatik hierfür zahlreiche und wesentliche Beiträge leisten. Mit über 20 Veröffentlichungen in internationalen Zeitschriften und Tagungsbänden mit kritischem Begutachtungsprozess und mit 5 abgeschlossenen Doktorarbeiten hat sich die Arbeitsgruppe wieder einen internationalen Spitzenplatz erarbeitet. Es ist ihr dadurch auch gelungen, von der Deutschen Forschungsgemeinschaft drei neue grundlagenorientierte Forschungsprojekte einzuwerben.

- ACCESS über die Verifikation, den Test und die Diagnose von Hardware-Infrastruktur
- OTERA-III über zuverlässiges rekonfigurierbares Rechnen
- PARSIVAL über die hochbeschleunigte und genaue Logik- und Fehlersimulation von integrierten Systemen mittels hochparalleler Prozessoren auf Grafikkarten.

Diese Forschungsschwerpunkte spiegeln sich auch in der Lehre wider, in der in Praktika, Seminaren und Vorlesungen die Studierenden an den Stand der Forschung herangeführt werden. An dieser Stelle möchte ich meinen Dank an alle Mitarbeiter des ITI ausdrücken, die dies mit großem persönlichen Einsatz möglich machen.

Stuttgart, März 2014

Hans-Joachim Wunderlich

Inhaltsverzeichnis

1. Institutsübersicht – Abteilung Rechnerarchitektur

1.1. Mitarbeiter

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sowie ca. 20 studentische Hilfskräfte in Forschung und Lehre

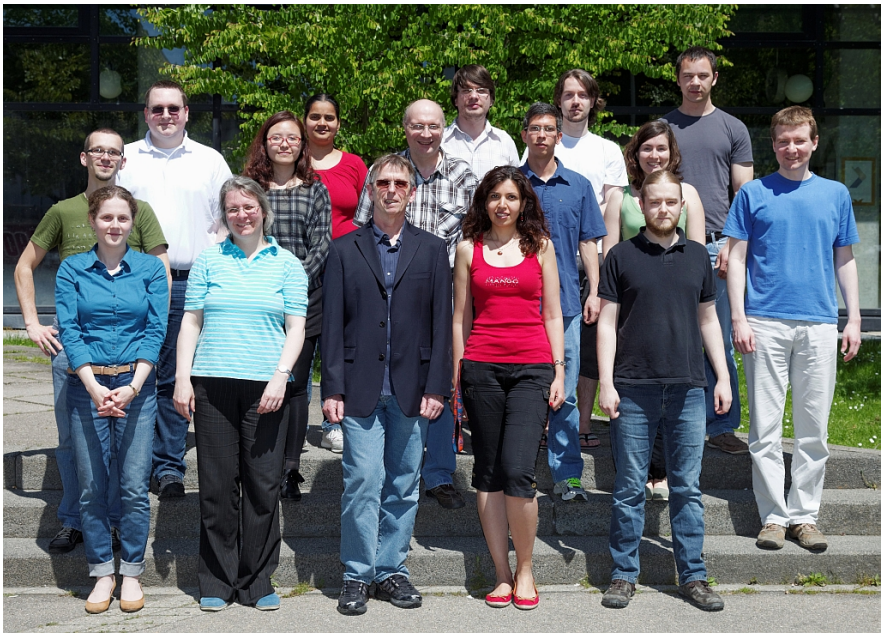

Bild unserer Mitarbeiter (Frühjahr 2014)

1.2. Forschungsschwerpunkte und Arbeitsgruppen

Ein großer Teil der Forschungsarbeiten erfolgt in enger Kooperation mit nationalen und internationalen Partnern aus Universitäten, Forschungseinrichtungen und der Industrie. Besondere Aufmerksamkeit wird auf Entwurfsmethoden und Hardwarestrukturen gelegt, mit denen hohe Anforderungen an Zuverlässigkeit, Sicherheit und Korrektheit der Systeme erfüllt werden können. In der Telekommunikation, Luft- und Raumfahrt, Verkehrs- oder Medizintechnik ist der Einsatz digitaler Systeme nur dann verantwortbar, wenn solche besonders hohen Qualitätsanforderungen eingehalten werden können. Mit Verfahren der Hardware-Verifikation wird versucht, die Korrektheit eines Entwurfs nachzuweisen, während beim Hardwaretest Fehler im gefertigten System gesucht werden. Fehlertoleranzverfahren sollen dafür sorgen, dass ein System auch bei Vorliegen eines Fehlers funktionsfähig bleibt oder zumindest nur sichere Zustände annimmt. Viele der hierbei verwendeten Methoden werden auch im Softwareentwurf eingesetzt und sind von allgemeiner Bedeutung in der Informatik.

1.2.1. Arbeitsgruppe Test

Bearbeiter:

M. Sc. Anusha Kakarala
Dipl.-Inf. Michael Kochte
M. Sc. Chang Liu
M. Sc. Abdullah Mumtaz
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Dipl.-Inf. Marcus Wagner

Die Arbeitsgruppe „Test“ beschäftigt sich mit dem Test digitaler mikroelektronischer Systeme. Dies umfasst die Modellierung komplexer Fehler, deren Simulation und die algorithmische Erzeugung von Teststimuli. Weiterhin erfordert eine kosteneffiziente Testdurchführung einen prüfgerechten Entwurf des Systems und seiner Komponenten.

Die Modellierung komplexer Fehler und Ableitung effizienter hochparalleler Simulations-Algorithmen sind aktuelle Forschungsthemen am Institut. Dabei werden Fehler auf unterschiedlichen Ebenen modelliert, so dass auch elektrische Effekte und Variationen berücksichtigt werden können. Die Alterung von Transistoren und Verbindungen im Chip erfordert auch einen effizienten Online-Selbsttest im Feld. In den Projekten OASIS und OTERA werden Online-Testverfahren und entsprechende Infrastruktur zur Testdurchführung in anwendungsspezifischen integrierten Schaltungen (ASICs) und rekonfigurierbaren FPGA-basierten Systemen entwickelt und analysiert, so dass Alterungseffekte während der Einsatzdauer der Systeme erkannt werden können. Zur Steuerung des Testablaufs und der Kommunikation auf dem Chip werden zunehmend rekonfigurierbare Scan-Ketten verwendet, deren Synthese und Verifikation im Projekt „ACCESS“ untersucht wird.

1.2.2. Arbeitsgruppe Zuverlässigkeit

Bearbeiter:

M. Sc. Rafał Baranowski
Dipl.-Inform. Claus Braun
M. Sc. Francesco Cervellera
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Dipl.-Inf. Alexander Schöll

Ebenenübergreifende Methoden zur Sicherung von Zuverlässigkeit und Verfügbarkeit digitaler Schaltungen und Rechnersysteme bilden den Forschungsschwerpunkt der Gruppe „Zuverlässigkeit“. Die Forschungsarbeiten reichen dabei von der Verifikation und dem Entwurf rekonfigurierbarer Zugriffsmechanismen nach der neuen Normierung IEEE 1687-2014 (Projekt ACCESS) über Entwurfsverfahren für robuste On-Chip-Kommunikation wie „Networks-on-a-Chip“ (Projekt ROCK)

und rekonfigurierbare Rechnerarchitekturen (Projekt OTERA) bis hin zur Absicherung von Algorithmen und Software auf höheren Ebenen. Auf der Softwareebene steht dabei die zuverlässige Beschleunigung wissenschaftlicher Anwendungen und Simulationen auf innovativen Many-Core-Prozessorarchitekturen und zukünftigen heterogenen, laufzeitrekonfigurierbaren Rechnerarchitekturen im Mittelpunkt (Projekt im Rahmen des Exzellenzclusters Simulation Technology). Weitere Forschungsschwerpunkte bilden die simulationsbasierte Vorhersage und Bewertung von Alterungsmechanismen in digitalen Schaltungen sowie der Entwurf digitaler Schaltungsstrukturen zur Überwachung der Alterung (Projekt OASIS).

1.2.3. Arbeitsgruppe Diagnose

Bearbeiter:

M. Sc. Alejandro Cook
Dipl.-Inf. Laura Rodríguez Gómez
Dipl.-Inf. Dominik Ull

Im Bereich Diagnose wurden Mehrfachfehler, Klassifikation transienter Fehler und Systemtest im Automobilbereich behandelt. Es folgt eine kurze Zusammenfassung der publizierten Arbeiten.

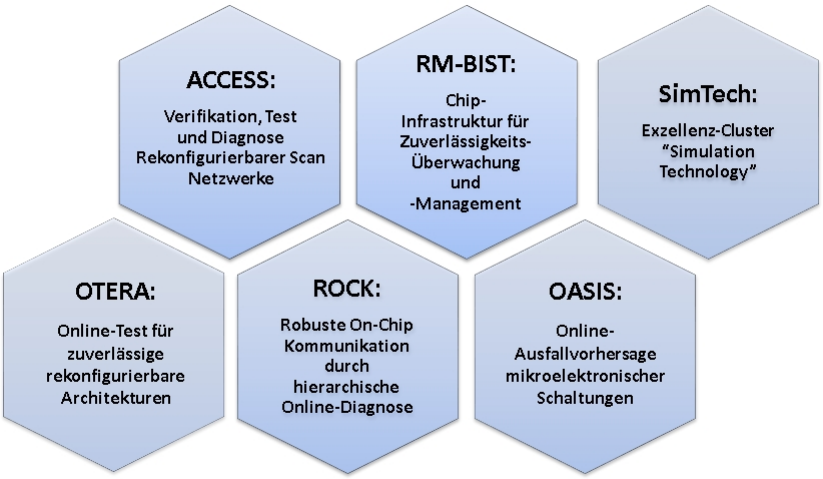
Defekte treten oft in Gruppen auf, so dass die Wahrscheinlichkeit eines Mehrfachfehlers signifikant höher ist als das Produkt der Auftrittswahrscheinlichkeiten der Einzelfehler. Diese Betrachtungsweise ist vorteilhaft zum Erreichen hoher Ausbeute, verkompliziert jedoch die Fehlerdiagnose. Mehrfachfehler treten besonders häufig beim Lernprozess, Yield Ramp-up oder bei der Analyse von Feldrückläufern auf. Es wurde ein Algorithmus zur Logikdiagnose erarbeitet, welcher robust gegenüber Mehrfachfehlern ist und diese mit hoher Genauigkeit diagnostizieren kann, auch bei komprimierten Testantworten, wie sie beim eingebetteten Test oder beim eingebauten Selbsttest auftreten. Der entwickelte Lösungsansatz verwendet die linearen Eigenschaften von MISR-Kompaktoren, um eine Fehlermenge zu identifizieren, welche mit großer Wahrscheinlichkeit die beobachteten fehlerhaften Signaturen erklärt. Experimente zeigen eine Verbesserung der Genauigkeit um bis zu 22% im Vergleich zu traditionellen Fehlerdiagnoseverfahren, die für vergleichbare Kompaktierungsraten geeignet sind.

Bei steigender transienter Fehlerrate ist die Unterscheidung zwischen intermittierenden und transienten Fehlern besonders herausfordernd. Relativ hohe transiente Fehlerraten treten nicht nur aufgrund von Partikeleinschlägen, sondern auch bei Architekturen für opportunistische Berechnung oder bei Technologien mit starken Variationen auf. Es wurde eine Methode zur Klassifizierung von Fehlern in permanente, intermittierende und transiente Fehler entwickelt. Diese Klassifikation basiert auf Zwischensignaturen, wie sie während der Durchführung eingebetteter Testverfahren oder eingebauter Selbsttests auftreten. Permanente Fehler sind leicht durch wiederholte Testdurchführungen zu erkennen. Intermittierende und transiente Fehler können in den meisten Fällen durch die Anzahl fehlerhafter Testdurchführungen identifiziert werden. Für die restlichen Fehler wurde eine

Bayessche Klassifikationsmethode erarbeitet, welche für große digitale Schaltungen einsetzbar ist. Die Kombination dieser Methoden ermöglicht die Erkennung intermittierender Fehler in 98% aller Fälle.

Die stark wachsende Zahl von Halbleitern in automobilen Systemen erhöht die Anzahl möglicher Defektmechanismen und vergrößert so den Aufwand, einen ausreichenden Grad an Qualität und Zuverlässigkeit zu erreichen. Ein vielversprechender Lösungsansatz stellt die Online-Durchführung struktureller Tests in Schlüsselkomponenten/Steuergeräten dar. Hierzu wurde eine optimierte Integration software-basierter Selbsttests (SBST) und eingebauter Selbsttests (BIST) in E/E-Architekturen vorgestellt. Dieser Ansatz integriert die Testdurchführung in einer nichtinvasiven Weise, d.h. (a) die Testdurchführung hat keine Auswirkungen auf funktionale Applikationen, und (b) benötigt keine kostenbehafteten Änderungen bestehender Kommunikationsabläufe, oder gar zusätzlichen Kommunikationsoverhead. Durch Untersuchung des Lösungsraums (design space exploration) wird eine Implementierung bestimmt, die optimal im Hinblick auf mehrere (teils gegensätzliche) Ziele wie Kosten, Sicherheit, Testqualität und Testzeit ist.

2. Projekte



2.1. ACCESS: Verifikation, Test und Diagnose Rekonfigurierbarer Scan-Netzwerke

seit 08.2014, DFG-Projekt: WU 245/17-1

Deutsche Forschungsgemeinschaft

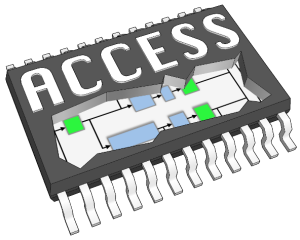
Projektmitarbeiter:

Dipl.-Inf. Michael Kochte
M. Sc. Chang Liu
Dipl.-Inf. Dominik Ull

Eingebettete Instrumente gewinnen zunehmend an Bedeutung und sind unerlässlich, um Skalierung und wachsende Komplexität aktueller Systeme-auf-einem-Chip (SoC) und Mikroprozessoren zu meistern. Chip-interne Instrumente werden sowohl bei der Produktion zur Verbesserung der Herstellung, Debug, Test und Diagnose, als auch im normalen Betrieb zur Felddiagnose und Instandhaltung eingesetzt. Rekonfigurierbare Scan-Netzwerke (RSN) stellen einen günstigen, allgemein einsetzbaren Zugriffsmechanismus für chip-interne Instrumente dar. Hierzu

sind bereits Standards verabschiedet (IEEE Std. 1149.1-2013 – JTAG-2013), oder in Vorbereitung (IEEE Std. P1687 – IJTAG). Sie beschreiben flexible Netzwerke aus Prüfpfaden, die verteilt konfigurierbar sind und Schnittstellen zur Integration eingebetteter Instrumente bereitstellen.

Effiziente Verifikations-, Test- und Diagnose-Methoden für RSN-Designs stellen aufgrund der kombinatorischen und sequentiellen Abhängigkeiten eine große Herausforderung dar. Diese Strukturen übersteigen die Möglichkeiten existierender Algorithmen, welche für konventionelle nicht-rekonfigurierbare Scan-Netzwerke, und allgemein beim Systementwurf eingesetzt werden. Im Projekt ACCESS werden skalierbare Methoden zur Entwurfsautomatisierung entwickelt, um die Einhaltung strenger Vorgaben für die Korrektheit, Zuverlässigkeit und Sicherheit von RSNs zu gewährleisten.



Die skalierbare formale Verifikation und Testerzeugung für erweiterte Scan-Netzwerke soll durch ein vereinheitlichtes Modell unterstützt werden. Darauf aufbauend werden Algorithmen zum formalen Beweis der Korrektheit von RSN-Designs und zum Nachweis nicht-funktionaler Eigenschaften, wie beispielsweise zur Sicherheit (“Safety” und “Security”), entwickelt. Spezialisierte Methoden zielen auf die Verifikation partieller Design-Spezifikationen in frühen Entwicklungsphasen ab. Die Testerzeugungs- und Diagnosealgorithmen berücksichtigen detaillierte Analysen der Fehlermechanismen in der Instrastruktur. Neue Techniken für den robusten Zugriff auch auf fehlerhafte Infrastruktur und deren partielle Nutzung werden die Post-Silicon-Validierung, die Systemdiagnose und die Ausbeutesteigerung unterstützen.

2.2. RM-BIST: Reliability Monitoring and Managing Built-In Self Test

seit 07.2012, DFG-Projekt: WU 245/13-1

DFG Deutsche Forschungsgemeinschaft

Projektmitarbeiter:

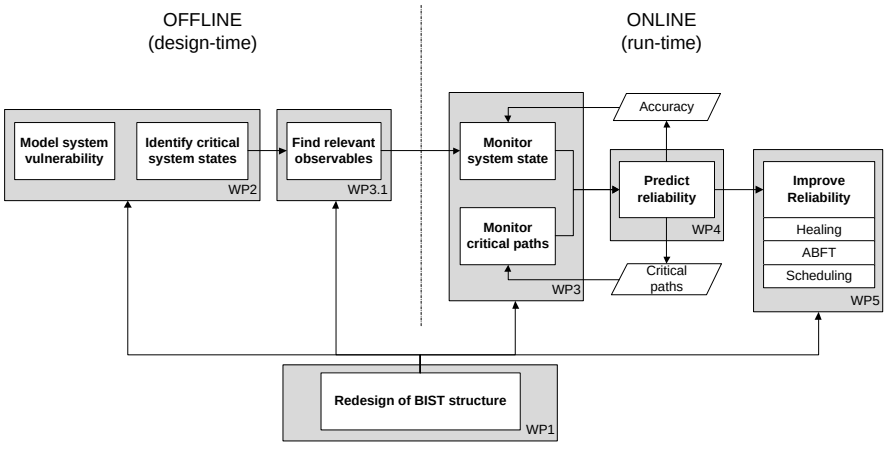
M. Sc. Rafał Baranowski
Dipl.-Inf. Michael Imhof
M. Sc. Alejandro Cook
M. Sc. Chang Liu

Kooperationspartner:

> Prof. Dr. Mehdi B. Tahoori, Chair of Dependable Nano Computing (CDNC)
> Karlsruhe Institute of Technology (KIT)

Das Hauptziel des RM-BIST Projekts ist es, die Test-Infrastruktur (Design for Test, DFT), die primär für den Produktionstest verwendet wird, zur Zuverlässigkeitsinfrastruktur (Design for Reliability, DFR) zu erweitern. Existierende Infrastruktur für den eingebetteten Selbsttest (Built-In Self-Test, BIST) wird durch geeignete Anpassungen während der Lebenszeit eines VLSI Systems wiederverwendet, um eine Systemüberwachung, die Identifikation kritischer Systemzustände und eine Vorhersage der Zuverlässigkeit zu ermöglichen. Zusätzlich wird die modifizierte Infrastruktur genutzt, um die Zuverlässigkeit gezielt zu steigern. Der zu entwickelnde Ansatz soll Fehler identifizieren und überwachen, welche die Systemzuverlässigkeit in verschiedenen Zeitskalen beeinflussen. Durch Prognostizierung sollen diese Fehler gleichzeitig abgemildert werden. Es werden unterschiedliche zuverlässigkeitsreduzierende Effekte behandelt, wie strahlungsinduzierte Soft Errors, intermittierende Fehler aufgrund von Prozess- und Laufzeitvariationen, Alterung von Transistoren und Elektromigration. Es ist das Ziel, eine Laufzeitunterstützung für die Überwachung und Steigerung der Zuverlässigkeit mittels Modifikation und Wiederverwendung existierender Infrastruktur für den eingebetteten Selbsttest unter minimalen Kosten bereitzustellen.

Im Rahmen von RM-BIST wurde eine nichtinvasive Überwachungsmethode entwickelt, die Alterungseffekte in digitalen Schaltungen anhand von Verhaltensmustern akkurat voraussagt. Zu diesem Zweck werden Verhaltensmuster sowie Betriebsbedingungen im Betrieb beobachtet. Die Alterungseffekte werden mittels maschineller Lernverfahren bestimmt. Dies ist eine neuartige Methode, die eine schnelle Voraussage über Alterungsraten im Betrieb ermöglicht.



2.3. ROCK: Robust Network On Chip Communication Through Hierarchical Online Diagnosis and Reconfiguration

since 08.2011, DFG-Project: WU 245/12-1

Deutsche Forschungsgemeinschaft

Project staff:

M. Sc. Atefe Dalirsani
Dipl.-Inf. Michael Imhof
M. Sc. Nadereh Hatami

Cooperation partner:

Prof. Dr.-Ing. Martin Radetzki, Institute of Computer Architecture and Computer Engineering
University of Stuttgart

The project ROCK targets the analysis and the prototypical development of robust architectures and associated design practices for Networks-on-Chips. Thereby, it meets the challenges of increased susceptibility of on-chip communication infrastructures against the massive influences caused by escalating integration density. ROCK pursues the strategy of conducting fault detection, online diagnosis and specific reconfiguration to tackle faults in a hierarchical manner throughout all network layers, aiming at selecting an optimal combination of activities over all layers.

In this year, the computer architecture group had three contributions covering the working packages of the project proposal. Firstly as a part of the first working package, we proposed a cross-layer modeling of the faults in the switches and links, which classifies the structural faults in the lower layers into a set of functional failure modes defined at the higher network layers. Classification quantifies the number of structural faults leading to each functional failure and thus is used to choose the optimum fault detection mechanism in a cross-layer manner.

Using this cross-layer fault modeling, we conducted a software-based self-test methodology with very high structural fault coverage while mitigating the test costs. Besides, this model is used for automatic functional test pattern generation. The generalized fault model, conditional line flip (CLF), has been employed to specify various kinds of structural faults at lower layers. Furthermore, the functional failure modes are defined with the input and output characteristic functions. The characteristic functions are extracted from the NoC switch specification. Therefore, the modeling is restricted neither to the faulty type nor to the switch structure.

The third contribution of this year was a concurrent error detection mechanism relying on the cross-layer fault detection idea. Toward this, we proposed a cross-layer synthesis approach using error detecting codes which guarantees concurrent detection of any single fault which produces an erroneous output. The synthesis approach outperforms conventional techniques for concurrent error detection.

2.4. OASIS: Online-Ausfallvorhersage mikroelektronischer Schaltungen mittels Alterungssignaturen

seit 03.2011, DFG-Projekt: WU 245/11-1

Projektmitarbeiter:

Dipl.-Inf. Michael Kochte
M. Sc. Rafał Baranowski
M. Sc. Nadereh Hatami
M. Sc. Chang Liu

Kooperationspartner:

Prof. Dr. Joachim N. Burghartz, Institut für Mikroelektronik Stuttgart (IMS)
Universität Stuttgart

Mechatronische Systeme, wie sie im Automobilbereich oder im industriellen Umfeld eingesetzt werden, benötigen zuverlässige mikroelektronische Lösungen, die mit zunehmender Miniaturisierung immer größeren Aufwand erfordern. Die zunehmende Verkleinerung von Strukturgrößen resultiert einerseits in einer steigenden Relevanz von physikalischen Alterungseffekten und andererseits in einem erhöhten Einfluss schwankender Technologieparameter auf die Lebensdauer. Die Lebensdauer mikroelektronischer Komponenten unterschreitet dabei mitunter die der mechanischen und elektromechanischen Bestandteile eines mechatronischen Systems.

Alterungsprozesse in mikroelektronischen Schaltungen hängen nicht nur von ihrer jeweiligen Auslastung, sondern auch stark von Fertigungsvariationen und den Umgebungsbedingungen wie beispielsweise der Temperatur und mechanischem Stress ab. Gängige statistische Verfahren zur Lebensdauerschätzung während der Entwicklung, der Fertigung und der Produktqualifizierung mittels Extrapolation minimal spezifizierter Betriebsdauern vernachlässigen diese individuellen Alterungseinflüsse. Sie können die zeitkontinuierliche Online-Überwachung des tatsächlichen Alters eines mikroelektronischen Systems nicht ersetzen.

Im Rahmen des OASIS-Projekts werden in Zusammenarbeit mit dem Institut für Mikroelektronik Stuttgart (IMS) Methoden entwickelt werden, um mittels Integration geeigneter Sensoren in aktiver Chipfläche eine zeitkontinuierliche Bestimmung (Online-Monitoring) des individuellen Lebensalters des mikroelektronischen Systems zu ermöglichen und rechtzeitig durch geeignete Konfiguration Ausfällen

vorbeugen zu können. Die Einbindung von Test- und Messstrukturen in den Halbleiterchip gestattet die Protokollierung sowohl der tatsächlichen Umgebungsbedingungen als auch unterschiedlicher alterungsbedingter Degradationseffekte.

Davon ungeachtet hängt die Lebensdauer mikroelektronischer Schaltungen auch stark von der Streuung kritischer Prozessparameter bei der Fertigung ab; sie definieren deren intrinsische Lebensdauer. Oben genannte Monitore müssen somit unabhängig von diesen Technologieschwankungen Zuverlässigkeitsinformationen liefern, die Rückschlüsse auf den Alterungs- und Gefährdungszustand einer Schaltung ermöglichen. Die gezielte Produktion von Technologiedurchläufen, die sich an den Grenzen des Fertigungsparameterraumes bewegen, und die Entwicklung und Durchführung von end-of-life Tests mit hohen Beschleunigungsfaktoren ermöglichen sowohl die Alterungsmodellierung als auch die Validierung der Monitorschaltungen.

Das Zusammenführen dieser Zuverlässigkeitsdaten in einer Monitoring-Infrastruktur, die Analyse von charakteristischen Alterungsmerkmalen unterschiedlicher Ausfallmechanismen und deren Gewichtung durch ein kumulatives Alterungsmodell erlauben eine Abschätzung des momentanen Alterungszustandes einer Schaltung.

Die Indikation des verbleibenden Lebensalters ermöglicht wirtschaftlichere systemtechnische Maßnahmen und Wartungskonzepte zur Steigerung der Zuverlässigkeit, wie beispielsweise die selbstindizierte Austauschaufforderung einzelner Komponenten oder das Zuhalten vorher ruhender Redundanzen.

2.5. OTERA: Online Test Strategies for Reliable Reconfigurable Architectures

seit 10.2010, DFG-Projekt: WU 245/10-1, 10-2, 10-3 DFG Deutsche Forschungsgemeinschaft

Projektmitarbeiter:

Dipl.-Inf. Michael Kochte
Dipl.-Inf. Michael Imhof
M. Sc. Francesco Cervellera
Dipl.-Inf. Eric Schneider

Kooperationspartner:

Prof. Dr.-Ing. Jörg Henkel, Chair for Embedded Systems (CES)
Karlsruhe Institute of Technology (KIT)

Das DFG-Schwerpunktprogramm 1500 „Design and Architectures of Dependable Embedded Systems - A Grand Challenge in the Nano Age“ erforscht effiziente Methoden zur Sicherung der Verlässlichkeit eingebetteter Systeme, die von der Schaltungs- bis zur Systemebene reichen. Im Rahmen dieses Schwerpunktprogramms untersucht das Institut für Technische Informatik Methoden des Online-Tests und der Zuverlässigkeitssteigerung für rekonfigurierbare Architekturen.

Dynamisch rekonfigurierbare Architekturen ermöglichen eine signifikante Beschleunigung unterschiedlichster Anwendungen durch Anpassung und Optimierung ihrer Hardware-Struktur zur Laufzeit. Der zuverlässige Betrieb dieser Architekturen wird jedoch durch permanente, intermittierende und transiente Fehler gefährdet. Dies umfasst latente Fehler, im Verlauf des Betriebs auftretende Fehler durch Alterung, sowie intermittierende und transiente Effekte (z.B. aufgrund hoher Temperatur, Strahlung, Schwankungen in der Stromversorgung, usw.).

寺 OTERA
Online Test Strategies for Reliable Reconfigurable Architectures

In der ersten Förderphase des OTERA-Projekts wurden permanente Fehler behandelt. Die zweite und dritte Förderphase zielen auf die Steigerung der Zuverlässigkeit rekonfigurierbarer Systeme zur Laufzeit durch den Einsatz von System-Monitoren, Verfahren zur Zuverlässigkeitsabschätzung und pro-aktiver Selbstverteidigungsmaßnahmen. Somit werden Beeinträchtigungen im Betrieb durch permanente, intermittierende und transiente Fehler minimiert. Dies wird durch die kontinuierliche Überwachung des Systems sowie die Abschätzung und Vorhersage des Systemzustands erreicht. Es werden basierend auf dem aktuellen und dem prognostizierten Systemzustand zuverlässigkeitssteigernde Maßnahmen bereitgestellt, die vom System zur Laufzeit ausgewählt und angewendet werden. Somit soll das System selbständig Betriebszustände finden, die die geforderte Leistung über die Lebensdauer gewährleisten ("guaranteed performability").

2.6. SimTech: Cluster of Excellence "Simulation-Technology": Mapping Simulation Algorithms to NoC MPSoC Computers

SimTech
Cluster of Excellence

since 06.2008, SimTech Cluster of Excellence

Project staff:

Dipl.-Inform. Claus Braun
Dipl.-Inf. Alexander Schöll

Since the beginning of the DFG Cluster of Excellence "Simulation Technology" (SimTech) at the University of Stuttgart in 2008, the Institute of Computer Architecture and Computer Engineering (ITI, RA) is an active part of the research within the Stuttgart Research Center for Simulation Technology (SRC SimTech). The institute's research includes the development of fault tolerant simulation algorithms for new, tightly-coupled many-core computer architectures like GPUs, the acceleration of existing simulations on such architectures, as well as the mapping of

complex simulation applications to innovative runtime reconfigurable heterogeneous computer architectures.

Within the research cluster, Hans-Joachim Wunderlich acts as a principal investigator (PI) and he co-coordinates the research activities of the SimTech Project Network PN2 "High-Performance Simulation across Computer Architectures". This project network is unique in terms of its interdisciplinary nature and its interfaces between the participating researchers and projects. Scientists from computer science, chemistry, physics and chemical engineering work together to develop and provide new solutions for some of the major challenges in simulation technology. The classes of computational problems treated within project network PN2 comprise quantum mechanics, molecular mechanics, electronic structure methods, molecular dynamics, Markov-chain Monte-Carlo simulations and polarizable force fields.

In the first phase of this project, Algorithm-Based Fault-Tolerance (ABFT) schemes have been modified and adapted to match the challenging characteristics of the many-core hardware. Simulation experiments based on structural fault injection have shown, that ABFT techniques for basic linear algebra operations are able to cover all detectable faults in the floating-point unit. Simulation algorithms from the fields of thermodynamics, microbiology, and quantum chemistry have been mapped to GPGPU architectures, with substantial speedups.

The second phase of the project concentrates on new methods that enable the direct mapping of simulation applications to innovative reconfigurable heterogeneous computer architectures. This includes the deduction and design of compute modules for an integrated software infrastructure to apply runtime load-balancing and adaption. A central aspect in this phase is the hardening of simulation algorithms against faults. Both, the tightly coupled, massively parallel architectures like GPGPUs and runtime reconfigurable architectures like FPGAs will be investigated to come up with centralized and decentralized fault tolerant control schemes.

3. Lehre

Die Abschlussarbeiten beziehen sich auf aktuelle Forschungen des Instituts sowie angeregte Themen unserer Kooperationspartner.

Das notwendige Hintergrundwissen wird durch eine Reihe von Vorlesungen, Seminaren und Praktika vermittelt, in denen die grundlegenden Strukturen und Design-Techniken sowie fortschrittliche Themen der Design-Automatisierung vorgestellt werden. Die Vorlesungen *Rechnerorganisation* und *Grundlagen der Rechnerarchitektur* geben einen Überblick über die Architektur moderner Datenverarbeitungssysteme und behandeln die grundlegenden Strukturen schneller digitaler Systeme. Außerdem werden in verschiedenen Seminaren Algorithmen und Strukturen für das Design von fehlertoleranten und zuverlässigen Systemen präsentiert.

Praktisches Knowhow erlernen die Studierenden in einem Praktikum für den Entwurf digitaler Systeme, dessen Ziel die Einführung in elementare elektronische Geräte ist und die Implementierung einfacher digitaler Schaltungen in FPGAs beinhaltet.

Die Abteilung Rechnerarchitektur bietet eine gleichnamige Vertiefungslinie an, die grundlegende Methoden des Entwurfs digitaler Systeme behandelt und innovative Rechnerstrukturen vorstellt.

3.1. Bachelor-Studiengang

3.1.1. Rechnerorganisation 1

Bachelor-Studiengang Informatik, Bachelor-Studiengang Softwaretechnik, Vorlesung mit Übungen, 3V + 1Ü SWS

Dozenten: H.-J. Wunderlich, E. Schneider, M. Wagner

Der moderne Rechnerentwurf geschieht auf mehreren Entwurfsebenen, angefangen vom Aufbau von Operations- und Steuerwerken aus einfachen logischen Gattern bis hin zum Entwurf von Befehlssätzen und der Unterstützung von Betriebssystemen. In der Vorlesung werden für alle Entwurfsebenen die heute gebräuchlichen Strukturkonzepte vorgestellt. Wegen der immer größer werdenden Komplexität digitaler Systeme spielt die Entwurfsmethodik eine wesentliche Rolle. Der Inhalt der Vorlesung wird im Rahmen von Gruppenübungen vertieft.

Die Vorlesung behandelt die folgenden Themenschwerpunkte:

- Einleitung

- Informationsdarstellung
- MIPS als RISC-Beispiel
- Operationswerke
- Steuerwerke
- Befehlszyklus und Unterbrechungen
- Pipelining und Scheduling
- Speicherorganisation
- Speicherverwaltung
- Betriebssysteme
- Eingabe und Ausgabe
- Leistungsbewertung

3.1.2. Rechnerorganisation 2 / Hardwarepraktikum

Bachelor-Studiengang Informatik, Vorlesung mit Übungen,
1V + 4Ü SWS

Dozenten: H.-J. Wunderlich, E. Schneider, D. Ull, M. Wagner

Rechnerorganisation 2 (auch "Hardwarepraktikum / HAPRA") ist eine 5 stündige Lehrveranstaltung im Studiengang Informatik, die praxisnah Grundlagen des Entwurfs digitaler Schaltungen und Systeme sowie den Zusammenhang zwischen Hard- und Software vermittelt. Die Veranstaltung gliedert sich in einen Praktikumsteil, in dem zwölf aufeinander aufbauende Versuche durchgeführt werden. Sie wird von einer wöchentlichen Vorlesung begleitet.

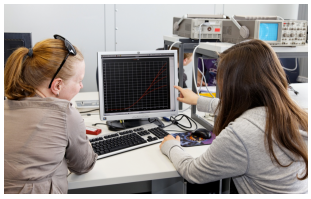
Datenverarbeitende Systeme werden heute in der Regel als digitale Schaltungen realisiert, wobei eine Vielzahl von Funktionseinheiten auf einem einzigen Chip integriert wird. Dabei sind eine Reihe von Schaltungsproblemen und Effekten zu berücksichtigen. Vor dem Einsatz integrierter Schaltungen im Hardwarepraktikum sollen daher die wesentlichen Bauelemente und einfache Grundschaltungen der Elektronik aufgebaut, ausgemessen und simuliert werden. Auf diese Weise werden Effekte und Probleme erfahrbar, die auch in integrierten Schaltungen auftreten.

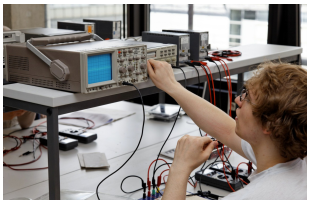
Anschließend wird ein einfacher RISC-Prozessor mithilfe kommerziellen Entwiklungswerkzeugen von Mentor Graphics und Xilinx entworfen und mit einem Field Programmable Gate Array (FPGA) in Hardware umgesetzt. Neben dem Entwurf kombinatorischer und sequentieller Schaltungen werden dabei auch Arbeitstechniken zur Komplexitätsbewältigung und Konzepte zur Schaltungsvalidierung vermittelt. Der selbst entworfene Prozessor wird am Ende des Praktikums in Maschinensprache programmiert.

Die Themen im Überblick:

- Grundlagen des Entwurfs digitaler Schaltungen und Systeme

- Aufbau und Ausmessung einfacher Grundschaltungen der Elektronik
- Modellierung und Simulation integrierter Schaltungen
- Entwurf eines einfachen RISC-Prozessor in VHDL
- Synthese und Test des Prozessorentwurfs mit FPGA Prototypen Boards
- Programmierung des Prozessors in Maschinensprache





Studierende im Hardwarepraktikum

3.1.3. Grundlagen der Rechnerarchitektur / Advanced Processor Architecture (in English)

Bachelor-Studiengang Informatik, Bachelor-Studiengang Softwaretechnik, Master-Studiengang Information Technology, Lecture and Exercises, 3L + 1E

Lecturer: H.-J. Wunderlich, R. Baranowski

This lecture covers advanced concepts in computer architecture. Beside classical concepts like processor design and manufacturing, performance evaluation and optimization, and computer arithmetic new trends are discussed like low power design. Low power design is essential in mobile computing and communication which is a dominating application of microprocessors.

Computation power is increasing by exploiting parallelism on all levels of computation. This course discusses instruction level parallelism, thread level parallelism, multiprocessor systems and emerging many-core technologies found in current graphic accelerators.

The lecture provides a solid background for the courses:

- Design & Test of Systems-on-a-Chip
- Hardware Verification
- Self-Testable Systems
- Fault Tolerant Systems

3.2. Master-of-Science- Studiengang

3.2.1. Hardware-based Fault Tolerance (in English)

Master-Studiengang Informatik, Master-Studiengang Softwaretechnik, Master-Studiengang Information Technology, Bachelor-Studiengang Informatik (Ergänzungsmodul), Lecture and Exercises, 3L + 1E

Lecturer: H.-J. Wunderlich, N. Hatami, M. Kochte

Micro- and Nano-electronic systems exhibit failures both right after production and during their operation. Systems for which safety and security is of concern have to be designed in a way that the desired function can be delivered even if some components fail or produce erroneous outputs. This lecture presents the most important techniques that allow to assess reliability of a system as well as to design fault tolerant systems.

The topics of the lecture are as follows:

- Terminology
- Measures of fault tolerance
- Techniques for structural and time redundancy
- Error detection and diagnosis
- Fault masking, repair, reconfiguration
- Fault-tolerant distributed systems

3.2.2. Design and Test of Systems on Chip (in English)

Master-Studiengang Informatik, Master-Studiengang Softwaretechnik, Master-Studiengang Information Technology, Lecture and Exercises, 2L + 2E

Lecturer: H.-J. Wunderlich, L. Rodríguez Gómez;
Analog and Mixed Signal Part by M. Berroth (INT)

Technological progress in designing and manufacturing integrated circuits allows the integration of complex microelectronic systems including processors, memory, application specific and analog circuits into a single chip. This trend dominates today's and future systems and their design process: Costly manual design of logic is replaced by a core-based design methodology.

Besides the different design styles, paradigms and standards the essential steps of automated design, test and programming of digital and mixed signal circuits are discussed. Exercises and labs serve to practice the use of commercial tools and designs.

In the lecture the following issues are addressed:

- Overview over system design
- Reuse and cores
- Standards and platforms
- Elements of analog and mixed signal designs
- Design validation and verification
- Test and design for testability with the related standards
- Application and programming of embedded processors

Prerequisites: Advanced Processor Architecture

3.2.3. Elements of High Performance RISC Processors (in English)

Master-Studiengang Informatik, Master-Studiengang Softwaretechnik, Master-Studiengang Information Technology, Exercises, 4E

Lecturer: R. Baranowski, L. Rodríguez Gómez

In this lab course a basic 32-bit RISC processor is extended with techniques common to high-performance processors.

The extensions include:

- Pipelining
- 4-way SIMD
- Pipelined hardware multiplier
- Cache, writeback queue, etc.

The resulting processor architecture is quite similar to the one used in the synergistic processing element of the Cell Broadband Engine, used e.g. in Playstation 3. In order to achieve high performance, proper design techniques and software tools for synthesis and analysis play an important role. The students learn how timing analysis, pipelining and retiming can be used to optimize the synthesis results. Finally, the processor is emulated on a Virtex-5 FPGA prototyping board.

The performance gain of the student's design is measured for the Mandelbrot set computation with respect to the basic RISC architecture. Because software has to be specifically tailored to high-performance processor architectures, the lab course also deals with scheduling techniques that avoid pipeline stalls.

3.2.4. Hardware Infrastructure for Safety and Security (in English)

Master-Studiengang Informatik, Master-Studiengang Softwaretechnik, Hauptseminar; Master-Studiengang Information Technology, Seminar,
2HS

Lecturer: H.-J. Wunderlich, C. Braun, A. Dalirsani, D. Ull

Application domains like automotive, avionics and medical engineering require high levels of safety and security. Failures in such safety-critical areas due to hardware malfunctions or attacks from the outside can lead to financial loss, and more important, to severe environmental harm, material damage, and loss of human life.

Ensuring safety and security of such electronic systems becomes increasingly harder as nano-scaled semiconductors are prone to variability and reliability-harming issues. The complexity of systems raises the possibilities of security vulnerabilities. Formally, safety is defined with respect to the consequences of system failures. When such a failure might lead to consequences that are determined to be unacceptable, the application is safety-critical. In essence, a system is safety-critical when we depend on it for our well being. The aim of safety-critical design is firstly to model the desired safety properties, and secondly to show that these properties are satisfied by design model implementations. Hardware security and protection against attacks from the outside is becoming more and more important. For instance, parts of the internal test infrastructure might be abused to gain access to digital systems for manipulation. Therefore, suitable design methods for hardware security are required.

This seminar deals with the most important aspects and the key challenges to assure safety and security in complex digital systems. We will discuss topics like Functional safety, Fault-tolerant hardware, Redundancy, Online testing, Hardware attacks and countermeasures, Design for trust, and Security of test infrastructure.

3.2.5. Data Mining and Machine Learning Approaches for Semiconductor Test and Diagnosis (in English)

Master-Studiengang Informatik, Master-Studiengang Softwaretechnik, Hauptseminar; Master-Studiengang Information Technology, Seminar,
2HS

Lecturer: H.-J. Wunderlich, A. Cook, L. Rodríguez Gómez, R. Baranowski, E. Schneider, D. Ull

New manufacturing issues at the nanoscale level lead to process variations, increased sensitivity to environmental conditions and degradation. These emerging challenges threaten both system quality and reliability, and make the exact behavior of semiconductor technology exceedingly hard to predict. Consequently, the test and diagnosis of complex VLSI systems need to evolve in order to account for performance uncertainty.

In order to fulfill this goal, semiconductor measurements may be analyzed, which characterize semiconductor performance during manufacturing and system-level tests. The extracted performance characteristics can used to improve a wide array of tasks in the semiconductor industry like, for example, analog diagnosis, yield optimization, adaptive test, system-level diagnosis, etc.

This challenge is a natural fit for data mining and machine learning approaches, which are best suited for problems where there is no fixed set of rules that can be efficiently specified in an algorithm. Instead, these techniques analyze different characteristics in the data itself and try to infer relationships among them.

This seminar deals with the most useful tools for data mining and machine learning for semiconductor test and diagnosis. We will discuss the principles and application of various techniques, such as regression, classification (support vector machines and neural networks), clustering and outlier detection.

3.3. Lehrveranstaltungen im Wintersemester 2013 - 2014

Titel	Veranstaltungsart	Dozent
Rechnerorganisation 1 3V	Vorlesung	H.-J. Wunderlich
Rechnerorganisation 1 1Ü	Übung	H.-J. Wunderlich E. Schneider M. Wagner
Hardware-Based Fault-Tolerance 3V	Vorlesung	H.-J. Wunderlich
Hardware-Based Fault-Tolerance 1Ü	Übung	H.-J. Wunderlich N. Hatami M. Kochte
Elements of High-Performance RISC Processors - Design and Synthesis 4Ü	Fachpraktikum	R. Baranowski L. Rodríguez Gómez
Hauptseminar: Hardware Infrastructure for Safety and Security 2HS	Hauptseminar	H.-J. Wunderlich Wiss. Mitarbeiter
Kolloquium Rechnerarchitektur 2K	Seminar	H.-J. Wunderlich Wiss. Mitarbeiter

3.4. Lehrveranstaltungen im Sommersemester 2014

Titel	Veranstaltungsart	Dozent
Rechnerorganisation 2 Hardwarepraktikum 1V	Vorlesung	H.-J. Wunderlich Wiss. Mitarbeiter
Rechnerorganisation 2 Hardwarepraktikum 4Ü	Übung	E. Schneider D. Ull M. Wagner H.-J. Wunderlich
Advanced Processor Architecture 3V	Vorlesung	H.-J. Wunderlich R. Baranowski
Advanced Processor Architecture 1Ü	Übung	R. Baranowski
Grundlagen der Rechnerarchitektur 3V	Vorlesung	H.-J. Wunderlich
Grundlagen der Rechnerarchitektur 1Ü	Übung	R. Baranowski
Design and Test of System on a Chip 2V	Vorlesung	H.-J. Wunderlich L. Rodríguez Gómez
Design and Test of System on a Chip 2Ü	Übung	L. Rodríguez Gómez
Seminar: Data Mining and Machine Learning Approaches for Semiconductor Test and Diagnosis 2HS	(Haupt-) Seminar	H.-J. Wunderlich R. Baranowski A. Cook L. Rodríguez Gómez E. Schneider D. Ull
Oberseminar Rechnerarchitektur 2K	Seminar	H.-J. Wunderlich Wiss. Mitarbeiter

3.5. Oberseminar

Im Rahmen des Oberseminars stellen Studierende und wissenschaftliche Mitarbeiterinnen und Mitarbeiter wesentliche Ergebnisse ihrer (Bachelor-, Master-, Diplom- und Doktor-) Arbeiten vor. In einem ca. halbstündigen Vortrag plus anschließender Diskussion werden die Kernpunkte der eigenen Arbeit und Leistung dargestellt.

Ein erfolgreich absolviertes Oberseminar ist zudem Voraussetzung, um am Institut eine Abschlussarbeit abzuschließen. Es folgt die Übersicht über die Vorträge des

Studienjahrs 2013 / 2014.

Accelerated Computation Using Runtime Partial Reconfiguration

M.Sc. cand. Naresh Nayak, Institut für Technische Informatik, 28.11.2013

Runtime reconfigurable architectures, which integrate a hard processor core along with a re- configurable fabric on a single device, allow to accelerate a computation by means of hardware accelerators implemented in the reconfigurable fabric. Runtime partial reconfiguration pro- vides the flexibility to dynamically change these hardware accelerators to adapt the computing capacity of the system. This thesis presents the evaluation of design paradigms which exploit partial reconfiguration to implement compute intensive applications on such runtime recon- figurable architectures. For this purpose, image processing applications are implemented on Zynq-7000, a System on a Chip (SoC) from Xilinx Inc. which integrates an ARM Cortex A9 with a reconfigurable fabric.

This thesis studies different image processing applications to select suitable candidates that benefit if implemented on the above mentioned class of reconfigurable architectures using runtime partial reconfiguration. Different Intellectual Property (IP) cores for executing basic image operations are generated using high level synthesis for the implementation. A software based scheduler, executed in the Linux environment running on the ARM core, is responsible for implementing the image processing application by means of loading appropriate IP cores into the reconfigurable fabric. The implementation is evaluated to measure the application speed up, resource savings, power savings and the delay on account of partial reconfiguration.

The results of the thesis suggest that the use of partial reconfiguration to implement an application provides FPGA resource savings. The extent of resource savings depend on the granularity of the operations into which the application is decomposed. The thesis could also establish that runtime partial reconfiguration can be used to accelerate the computations in reconfigurable architectures with processor core like the Zynq-7000 platform. The achieved computational speed-up depends on factors like the number of hardware accelerators used for the computation and the used reconfiguration schedule. The thesis also highlights the power savings that may be achieved by executing computations in the reconfigurable fabric instead of the processor core.

Pieceweise evaluation of Non-functional parameters

M. Sc. Nadereh Hatami, Institut für Technische Informatik, 12.12.2013

Non-Functional Properties (NFPs) are usually defined formally as mathematical equations. As environmental changes have significant effect on NFPs during the lifetime of the circuit, accurate NFP prediction demands frequent evaluation of relevant NFP models. In this talk, Piecewise evaluation technique for NFP prediction is presented to find a trade-off between the frequency of evaluations and the accuracy of NFP prediction.

Incremental Computation of Delay Fault Detection Probability for Variation-Aware Test Generation

Dipl.-Inf. Marcus Wagner, Institut für Technische Informatik, 19.12.2013

Large process variations in recent technology nodes present a major challenge for the timing analysis of digital integrated circuits. The optimization decisions of a statistical delay test generation method must therefore rely on the probability of detecting a target delay fault with the currently chosen test vector pairs. However, the huge number of probability evaluations in practical applications creates a large computational overhead.

To address this issue, this paper presents the first incremental delay fault detection probability computation algorithm in the literature, which is suitable for the inner loop of automatic test pattern generation methods. Compared to Monte Carlo simulations of NXP benchmark circuits, the new method consistently shows a very large speedup and only a small approximation error.

Delay Characterization in FPGA-based Reconfigurable Systems

M.Sc. cand. Shihao Zhang, Institut für Technische Informatik, 19.12.2013

Runtime reconfigurable architectures accelerate the operation of a standard processor core by hardware accelerators implemented in reconfigurable gate arrays (FPGAs). This allows for high flexibility and dynamic adaptation of the computational capacity of the system. Manufactured in latest technologies at 28 nm, concerns rise about the impact of aging related failure mechanisms. To detect degradation in the reconfigurable gate arrays, dedicated on- and offline test methods must be employed in the field. In this thesis, we develop and evaluate delay test and characterization methods for the FPGA-based runtime part of the system. This comprises the generation of special test configurations and test and characterization infrastructure on the FPGA such that transition delay along certain paths can be measured at high accuracy.

Challenges in Post-Silicon Validation

Dipl.-Inf. Laura Rodríguez Gómez, Institut für Technische Informatik, 23.01.2014

Post-silicon validation is the last step for a semiconductor device before manufacturing. As the last phase before production, it offers the last opportunity to detect bugs which, if discovered after production, would mean long time and high costs to correct. While other phases of design and production such as pre-silicon validation and manufacturing test have been widely explored and mature techniques exist to overcome their problems, post-silicon validation still poses some challenges. In this talk a survey of existing techniques will be given as a starting point for discussion about open problems in post-silicon validation.

Exploiting Information and Hardware Redundancy for Area-Aware Concurrent error Detection in Network-on-Chips

M.Sc. Atefe Dalirsani, Institut für Technische Informatik, 06.02.2014

Error detecting codes are used for concurrent error detection (CED) specially in the safety critical applications, to detect permanent and transient faults during normal operation of the circuit. In the Network-on-Chip (NoC), as data transmission medium of many core SoCs, data encoding using error detecting codes in combination with data retransmission are typically used to detect and correct the errors on the transmitted data during system's mission mode. However, a portion of NoC switch logic is dedicated to manage the flow of data, for example routing algorithm, scheduling, and congestion control. Concurrent error detection (CED) scheme must have a solution for the faults in this part as well. By incorporating the data encoding concept and the self-checking designs using error detecting codes, we develop a self-checking switch which is able to detect the erroneous behavior due to any single combination and transition fault, irrespective of its permanent, transient and intermittent nature.

Machine Learning Methods for Fault Classification

M. Sc. cand. Siddharth Sunil Gosavi, Institut für Technische Informatik, 08.05.2014

With the constant evolution and ever-increasing transistor densities in semiconductor technology, error rates are on the rise. Errors that occur on semiconductor chips can be attributed to permanent, transient or intermittent faults.

Out of these errors, once permanent errors appear, they do not go away and once intermittent faults appear on chips, the probability that they will occur again is high, making these two types of faults critical. Transient faults occur very rarely, making them non-critical. Incorrect classification during manufacturing tests in case of critical faults, may result in failure of the chip during operational lifetime or decrease in product quality, whereas discarding chips with non-critical faults may result in unnecessary yield loss.

Existing mechanisms to distinguish between the fault types are mostly rule-based, and as fault types start manifesting similarly as we move to lower technology nodes, these rules become obsolete over time. Hence, rules need to be updated every time the technology is changed.

Machine learning approaches have shown that the uncertainty can be compensated with previous experience. In our case, the ambiguity of classification rules can be compensated by storing past classification decisions and 'learn' from those for accurate classification.

This thesis presents an effective solution to the problem of fault classification in VLSI chips using Support Vector Machine (SVM) based machine learning techniques.

Integration von algorithmenbasierter Fehlertoleranz in grundlegenden Operationen der Linearen Algebra auf GPGPUs

Dipl.-Inf. cand. Sebastian Halder, Institut für Technische Informatik, 08.05.2014

Der Einsatz algorithmenbasierter Fehlertoleranz bietet eine Möglichkeit, auftretende Fehler bei Operationen der linearen Algebra zu erkennen, zu lokalisieren und zu korrigieren. Diese Operationen der linearen Algebra können durch den Einsatz hochoptimierter Bibliotheken mit einem großen Geschwindigkeitszuwachs gegenüber Mehrkernprozessoren auf GPGPUs ausgeführt werden. Die Integration der algorithmenbasierter Fehlertoleranz unter Verwendung dieser Bibliotheken für einige ausgewählte Operationen der linearen Algebra ist Kern dieser Arbeit.

Bei der Überprüfung der Ergebnisse auf aufgetretene Fehler müssen dabei Werte verglichen werden, die durch einen Rundungsfehler behaftet sind und somit nicht mit einem Test auf Gleichheit abgeprüft werden können. Deshalb werden Fehlerschwellwerte benötigt, bei deren Überschreitung ein Fehler erkannt und anschließend korrigiert werden kann.

In dieser Arbeit wurden deterministische Methoden zur Fehlerschwellwertbestimmung untersucht und eine probabilistische Methode zur Fehlerschwellwertbestimmung entwickelt. Diese wurden anhand experimenteller Untersuchungen bezüglich der Qualität im Sinne der Differenz zum real aufgetretenen Rundungsfehler, der Fehlererkennung bei Fehlerinjektion und der Performanz der Methoden bei Implementierung auf GPGPUs miteinander verglichen. Die probabilistische Methode zeichnet sich dabei durch einen näher am Rundungsfehler liegenden Fehlerschwellwert aus, ist dadurch in der Lage einen größeren Anteil auftretender Fehler zu erkennen und kann ohne großen Mehraufwand auf GPGPUs implementiert werden.

Preliminary Timing Correlation Analysis for Effective Observation Point Selection

M.Sc. Chang Liu, Institut für Technische Informatik, 15.05.2014

Aggressive technology scaling comes along with increasing parameter variations and a growing susceptibility to transistors aging. The process variation as well as aging degradation cause a parameter shift of transistors and interconnects. This generates a large spread in the critical path delay of integrated circuits. As a result, recently path delay monitoring schemes are intensively studied. Stability checkers (SC) are a well-known and commonly utilized approach to detect timing violations due to accumulating delay increase along paths. State-of-the-art methods often place the delay monitor at the end of some critical and long paths. However, due to the significant hardware penalty including global wiring, sometimes the circuit designers still have to face the dilemma of balancing the trade-off between overhead and observability. Additionally, the low sensitization ratio of certain functional applications may lead to large testing latencies or even an unmonitored delay violation progress.

In this work, we propose a stability checker placement/relocation method by analyzing the timing correlation between outputs and intermediate circuit nodes. In-

stead of integrating sensors only in flip-flops (FF), the stability checkers are inserted at meticulously selected positions in the circuit, named as observation points (OPs). The preliminary experimental results show the effectiveness and efficiency of the proposed methodology.

Improving the Accuracy of Fundamental Statistical Timing Analysis Operations

Dipl.-Inf. Marcus Wagner, Institut für Technische Informatik, 26.06.2014

Parameter variations have emerged as one of the most important challenges for the statisical timing analysis of modern digital integrated circuits. Both circuit design and delay test optimization have to rely on a large number of accurate predictions of the circuit timing behaviour. Recently proposed circuit optimization and statistical delay test generation methods are therefor guided by the distribution of the greatest transition path delay, which provides vital information about the delay test quality and the yield loss. However, previous approaches to approximate the distribution of the maximum delay have been limited by high computational effort or low accuracy.

To address this problem, this talk presents a generalization of Clark's maximum approximation method which preserves the skewness of all intermediate result distributions. The experimental results show a significant reduction of the approximation error.

OASIS Testchip Gateway (INFOTECH Study Project)

M.Sc. cand. Julian Oberacker, Institut für Technische Informatik, 03.07.2014

Microelectronic circuits are aging during their operation. A testchip was designed to study aging effects and sensor mechanisms on an experimental basis. An array of daisy-chained chips will be operated in a harsh environment to speed up aging. During the aging process, continuous test shall show the impact of wear-out effects and prove the capability to detect those effects before the circuits fail.

The experiments shall be configurable and programmable with a workstation. To be able to interface with the testchips, a gateway between workstation and chips under test is necessary.

The task of this study thesis is to design and implement the gateway and the application interface for the workstation software.

Structural Software-Based Self-Test Generation for Complex Pipelines

Dipl.-Inf. Dominik Ull, Institut für Technische Informatik, 17.07.2014

Increasing functionality and performance requirements demand high-performance microprocessor designs to comprise complex pipeline structures. For throughput optimization and hazard resolution, these pipelines contain bypass and hard-to-test forwarding logic.

We propose an automated software-based self-test (SBST) generation method, which directly targets hard-to-test pipeline forwarding logic. Topological information from the target's register-transfer-level (RTL) description is used to construct a reduced combinational circuit model at gate-level. Test programs are generated by means of structural automatic test pattern generation (ATPG). Required constraints are automatically extracted from the processor's hardware description. Experiments with an industrial processor pipeline show significant improvements in stuck-at fault coverage (+4.2%), when compared to test generation methods, that do not explicitly target forwarding logic. Overall, a fault coverage of 95.5% is achieved.

3.6. Dissertationen

Bearbeiter	Thema
Rafał Baranowski	Reconfigurable Scan Networks: Formal Verification, Access Optimization and Protection
Nadereh Hatami	Multi Level Analysis of Non-Functional Properties
Christian G. Zöllin	Test Planning for Low-Power Built-In Self Test
Michael A. Kochte	Boolean Reasoning for Digital Circuits in Presence of Unknown Values: Application to Test Automation
Alejandro Cook	In-Field Structural Methods for End-to-End Automotive Digital Diagnosis

3.6.1. Rafał Baranowski: Reconfigurable Scan Networks: Formal Verification, Access Optimization and Protection

M. Sc. Rafał Baranowski: Reconfigurable Scan Networks: Formal Verification, Access Optimization and Protection

Hauptberichter: Prof. Dr. rer. nat. habil. Hans-Joachim Wunderlich
Mitberichter: Prof. Dr.-Ing. Wolfgang Kunz, Technische Universität Kaiserslautern
Prüfung: 07.01.2014
Publikationsdatum: 14.03.2014

Abstract:

To facilitate smooth VLSI development and improve chip dependability, VLSI designs incorporate instrumentation for post-silicon validation and debug, volume test and diagnosis, as well as in-field system maintenance. Examples of on-chip instruments include embedded logic analyzers, trace buffers, test and debug controllers, assertion checkers, and physical sensors, to name just a few. Since the amount of embedded instrumentation in system-on-a-chip designs increases at an exponential rate, scalable mechanisms for instrument access become indispensable.

Reconfigurable scan architectures emerge as a suitable mechanism for access to on-chip instruments. Such structures integrate embedded instrumentation into a common scan network together with configuration registers that determine how data are transported through the network. For test purposes, the design of regular reconfigurable scan networks is covered by IEEE Std. 1149.1-2013 (Joint Test Action Group, JTAG) and IEEE Std. 1500 (Standard for Embedded Core Test, SECT). For general-purpose instrumentation, the ongoing standardization effort IEEE P1687 (Internal JTAG, IJTAG) allows user-defined scan architectures with arbitrary access control.

The flexibility of reconfigurable scan networks poses a serious challenge: The deep sequential behavior, limited serial interface, and complex access dependencies are beyond the capabilities of state-of-the-art verification methods. This thesis contributes a novel modeling method for formal verification of reconfigurable scan architectures. The proposed model is based on a temporal abstraction which is both sound and complete for a wide array of scan networks. Experimental results show that this abstraction improves the scalability of model checking algorithms tremendously.

The access to instruments in complex reconfigurable scan networks requires specialized algorithms for pattern generation. This problem is addressed with formal techniques that leverage the temporal abstraction to generate valid access patterns with low access time. This work presents the first method applicable to pattern retargeting and access merging in complex reconfigurable architectures compliant with IEEE Std. P1687.

Embedded instrumentation is an integral system component that remains functional throughout the lifetime of a chip. To prevent harmful activities, such as tampering with safety-critical systems, and reduce the risk of intellectual property infringement, the access to embedded instrumentation requires protection. This thesis provides a novel, scalable protection for general reconfigurable scan networks. The proposed method allows fine-grained control over the access to individual instruments at low hardware cost and without the need to redesign the scan architecture.

3.6.2. Nadereh Hatami: Multi Level Analysis of Non-Functional Properties

M. Sc. Nadereh Hatami: Multi Level Analysis of Non-Functional Properties

Hauptberichter: Prof. Dr. rer. nat. habil. Hans-Joachim Wunderlich
Mitberichter: Prof. Paolo Ernesto Prinetto, Politecnico di Torino
Prüfung: 14.03.2014
Publikationsdatum: 14.05.2014

Abstract:

System properties are usually classified into functional (behavioral) and non-functional properties (NFPs). While functional properties refer to system behavior, NFPs are attributes, or constraints of a system. Power dissipation, temperature

distribution on the chip, vulnerability to soft and intermittent errors, reliability and robustness are all examples of NFPs.

The exponential increase of system complexity and the transistor's smaller feature sizes pose new challenges to functional as well as non-functional properties of the system. Therefore, it becomes more important to understand and model their impact at early design phases.

This work targets dynamic, quantifiable NFPs and aims at providing a basis for the accurate analysis of this class of NFPs at early design phases. It proposes an accurate and efficient NFP characterization and analysis method for complex embedded systems. An efficient NFP prediction method helps designers understand how the devices behave over time, identify NFP bottlenecks within circuits and make design trade-offs between performance and different NFPs in the product design stage. It assists manufacturers build their circuits such that no performance degradation due to specific NFPs dominate over the life of an operating device.

The developed methodology is based on an efficient multi-level system-wide simulation that considers the target system application. High NFP evaluation speed is achieved using a novel piecewise evaluation technique which splits the simulation time into evaluation windows and efficiently evaluates NFP models once per window by partial linearization. The piecewise evaluation method is a fast, yet accurate replacement for a cycle-accurate NFP evaluation. To consider the mutual impact of different NFPs on each other, all NFP models are integrated into a common evaluation framework. The effect of some positive or negative feedback between different NFPs is dynamically considered during simulation. Evaluations are based on target applications instead of corner case analysis to provide a realistic prediction.

The contributions of this work can be summarized as follows:

(1) Generality: This work proposes a holistic, scalable NFP prediction methodology for multiple, interdependent NFPs. The NFP simulation and evaluation method is independent of a specific NFP, a particular model or a specific system or core. In addition, the method allows for multiple designs under analysis and multiple NFPs. As soon as the system is available at transaction level, it can be used for NFP estimation.

(2) Speed up: The NFP-aware simulation is performed on a multi-level platform while low level simulation is accelerated using parallelism. The complete system simulation is always kept at transaction level. All the NFPs under analysis can be estimated with a single simulation run. In addition, the evaluation speed can be increased by increasing the size of the evaluation window.

(3) Accuracy: The accuracy is a function of the accuracy of the selected model and the evaluation methodology. This work provides a method for integrating arbitrary low-level models into the system analysis. The right choice of low-level models may depend on the requirements for accuracy and efficiency. To preserve the low level evaluation accuracy, the required observables for piecewise evaluation are obtained at low level. The evaluation accuracy for the piecewise approach can be adjusted by calibrating the window size. Besides, rather than using statistical or

worst-case analysis techniques (which may be too pessimistic in case of embedded systems with well defined applications), the complete system is simulated with the target applications and actual workloads to obtain higher accuracy for specific applications.

3.6.3. Christian G. Zöllin: Test Planning for Low-Power Built-In Self Test

Dipl.-Ing. Christian G. Zöllin: Test Planning for Low-Power Built-In Self Test

Hauptberichter: Prof. Dr. rer. nat. habil. Hans-Joachim Wunderlich
Mitberichter: Prof. Dr. Ilia Polian, Universität Passau
Prüfung: 16.05.2014
Publikationsdatum: 15.01.2015

Abstract:

Power consumption has become the most important issue in the design of integrated circuits. The power consumption during manufacturing or in-system test of a circuit can significantly exceed the power consumption during functional operation. The excessive power can lead to false test fails or can result in the permanent degradation or destruction of the device under test. Both effects can significantly impact the cost of manufacturing integrated circuits.

This work targets power consumption during Built-In Self-Test (BIST). BIST is a Design-for-Test (DFT) technique that adds additional circuitry to a design such that it can be tested at-speed with very little external stimulus. Test planning is the process of computing configurations of the BIST-based tests that optimize the power consumption within the constraints of test time and fault coverage.

In this work, a test planning approach is presented that targets the Self-Test Using Multiple-input signature register and Parallel Shift-register sequence generator (STUMPS) DFT architecture. For this, the STUMPS architecture is extended by clock gating in order to leverage the benefits of test planning. The clock of every chain of scan flip-flops can be independently disabled, reducing the switching activity of the flip-flops and their clock distribution to zero as well as reducing the switching activity of the down-stream logic. Further improvements are obtained by clustering the flip-flops of the circuit appropriately.

The test planning problem is mapped to a set covering problem. The constraints for the set covering are extracted from fault simulation and the circuit structure such that any valid cover will test every targeted fault at least once. Divide-and-conquer is employed to reduce the computational complexity of optimization against a power consumption metric. The approach can be combined with any fault model and in this work, stuck-at and transition faults are considered.

The approach effectively reduces the test power without increasing the test time or reducing the fault coverage. It has proven effective with academic benchmark circuits, several industrial benchmarks and the Synergistic Processing Element (SPE) of the Cell/B.E.™Processor [Riley et al., 2005]. Hardware experiments have been

conducted based on the manufacturing BIST of the Cell/B.E.™Processor and shown the viability of the approach for industrial, high-volume, high-end designs.

In order to improve the fault coverage for delay faults, high-frequency circuits are sometimes tested with complex clock sequences that generate test with three or more at-speed cycles (rather than just two of traditional at-speed testing). In order to allow such complex clock sequences to be supported, the test planning presented here has been extended by a circuit graph based approach for determining equivalent combinational circuits for the sequential logic.

In addition, this work proposes a method based on dynamic frequency scaling of the shift clock that utilizes a given power envelope to it full extent. This way, the test time can be reduced significantly, in particular if high test coverage is targeted.

3.6.4. Michael A. Kochte: Boolean Reasoning for Digital Circuits in Presence of Unknown Values: Application to Test Automation

Dipl.-Inf. Michael A. Kochte: Boolean Reasoning for Digital Circuits in Presence of Unknown Values: Application to Test Automation

Hauptberichter: Prof. Dr. rer. nat. habil. Hans-Joachim Wunderlich
Mitberichter: Prof. Xiaoqing Wen, Ph.D., Kyushu Institute of Technology
Prüfung: 22.05.2014
Publikationsdatum: 27.06.2014

Abstract:

The exponential growth in digital VLSI design scale and complexity has been enabled by comprehensive adoption of design automation tools. In the digital domain, design automation from design entry over synthesis, validation, verification to test preparation is based on reasoning about logic functions and their manipulation.

Limited knowledge about the circuit behavior may require that nodes in the circuit are modeled as having an unknown value, for instance when using incompletely specified design models. Circuit nodes also need to be modeled as unknown if their values cannot be controlled during operation or test, or if their value during operation is not known at the time of modeling.

To reflect such unknown values in design automation tools, the algorithms typically employ logic algebras with a special symbol 'X' denoting the unknown value. However, the reasoning about functions based on such algebras results in an overestimation of unknown values in the model, and an accurate or optimal solution cannot be found. This pessimism in presence of unknown values causes additional costs at different stages of the design and test process and may even reduce product quality.

This work proposes novel, efficient approximate and accurate algorithms for the analysis of the behavior of digital circuits in presence of unknown values. Heuristics and formal Boolean reasoning techniques are combined to achieve short runtimes. The algorithms allow accurate logic and fault simulation as well as accurate

automatic test pattern generation in presence of unknown values. The implications to the overhead and effectiveness of design-for-test structures are studied. The proposed algorithms are the first to completely overcome the pessimism of conventional algorithms found in today's VLSI design automation tools also for larger circuits.

Experiments on benchmark and industrial circuits investigate the pessimism in conventional algorithms and show the increased accuracy achieved by the proposed algorithms. The results demonstrate the benefits of approximate and accurate reasoning in different applications in the VLSI design process, especially in the test automation domain.

3.6.5. Alejandro Cook: In-Field Structural Methods for End-to-End Automotive Digital Diagnosis

M. Sc. Alejandro Cook: In-Field Structural Methods for End-to-End Automotive Digital Diagnosis

Hauptberichter: Prof. Dr. rer. nat. habil. Hans-Joachim Wunderlich
Mitberichter: Prof. Dr.-Ing. Jürgen Teich, Friedrich-Alexander-Universität, Erlangen-Nürnberg
Prüfung: 16.07.2014
Publikationsdatum: 03.09.2014

Abstract:

The automotive domain has strongly relied on recent advances in semiconductor technology in order to offer customers a huge amount of appealing features of overwhelming complexity. As traditional functional tests are no longer sufficient to fulfill automotive diagnostic requirements, the analysis of automotive semiconductor failures has become a major quality concern. Semiconductor structural test solutions are already key technologies for the successful manufacturing of any integrated circuit. However, these techniques place stringent constraints on the test application process, which cannot be easily enforced outside the manufacturing environment. The methods and algorithms in this dissertation enable the introduction of structural test and diagnostic solutions into the failure analysis process of the automotive industry.

3.7. Diplomarbeit

3.7.1. Sebastian Halder: Integration von algorithmenbasierter Fehlertoleranz in grundlegenden Operationen der Linearen Algebra auf GPGPUs

Betreuer: Dipl.-Inform. Claus Braun, Dipl.-Inf. Alexander Schöll

Abgabedatum: 17.04.2014

Kurzfassung:

Der Einsatz algorithmenbasierter Fehlertoleranz bietet eine Möglichkeit, auftretende Fehler bei Operationen der linearen Algebra zu erkennen, zu lokalisieren und zu korrigieren. Diese Operationen der linearen Algebra können durch den Einsatz hochoptimierter Bibliotheken mit einem großen Geschwindigkeitszuwachs gegenüber Mehrkernprozessoren auf GPGPUs ausgeführt werden. Die Integration der algorithmenbasierten Fehlertoleranz unter Verwendung dieser Bibliotheken für einige ausgewählte Operationen der linearen Algebra ist Kern dieser Arbeit.

Bei der Überprüfung der Ergebnisse auf aufgetretene Fehler müssen dabei Werte verglichen werden, die durch einen Rundungsfehler behaftet sind und somit nicht mit einem Test auf Gleichheit abgeprüft werden können. Deshalb werden Fehlerschwellwerte benötigt, bei deren Überschreitung ein Fehler erkannt und anschließend korrigiert werden kann.

In dieser Arbeit wurden deterministische Methoden zur Fehlerschwellwertbestimmung untersucht und eine auf einer probabilistische Methode zur Abschätzung des Rundungsfehlers basierende Methode zur Fehlerschwellwertbestimmung angepasst und weiterentwickelt. Diese Methoden zur Fehlerschwellwertbestimmung wurden anhand experimenteller Untersuchungen bezüglich der Qualität im Sinne der Differenz zum gemessenen Rundungsfehler, der Fehlererkennungsraten bei Fehlerinjektion und der Performanz der Methoden bei Implementierung auf GPGPUs miteinander verglichen. Die probabilistische Methode zeichnet sich dabei durch einen näher am auftretenden Rundungsfehler liegenden Fehlerschwellwert aus, ist dadurch in der Lage einen größeren Anteil auftretender Fehler zu erkennen und zeigt eine hohe Performanz bei der Verwendung auf GPGPUs.

3.8. Master-Arbeiten

Bearbeiter	Betreuer	Thema
Naresh Nayak	Michael Kochte Michael Imhof	Accelerated Computation Using Runtime Partial Reconfiguration
Shihao Zhang	Michael Kochte Michael Imhof	Delay Characterization in FPGA-based reconfigurable Systems
Siddharth Sunil Gosavi	Laura Rodríguez Gómez	Machine Learning Methods for Fault Classification

3.8.1. Naresh Nayak: Accelerated Computation Using Runtime Partial Reconfiguration

Betreuer: Dipl.-Inf. Michael Kochte, Dipl.-Inf. Michael Imhof

Abgabedatum: 26.11.2013

Abstract:

Runtime reconfigurable architectures, which integrate a hard processor core along with a re- configurable fabric on a single device, allow to accelerate a computation by means of hardware accelerators implemented in the reconfigurable fabric. Runtime partial reconfiguration provides the flexibility to dynamically change these hardware accelerators to adapt the computing capacity of the system. This thesis presents the evaluation of design paradigms which exploit partial reconfiguration to implement compute intensive applications on such runtime reconfigurable architectures. For this purpose, image processing applications are implemented on Zynq-7000, a System on a Chip (SoC) from Xilinx Inc. which integrates an ARM Cortex A9 with a reconfigurable fabric.

This thesis studies different image processing applications to select suitable candidates that benefit if implemented on the above mentioned class of reconfigurable architectures using runtime partial reconfiguration. Different Intellectual Property (IP) cores for executing basic image operations are generated using high level synthesis for the implementation. A software based scheduler, executed in the Linux environment running on the ARM core, is responsible for implementing the image processing application by means of loading appropriate IP cores into the reconfigurable fabric. The implementation is evaluated to measure the application speed up, resource savings, power savings and the delay on account of partial reconfiguration.

The results of the thesis suggest that the use of partial reconfiguration to implement an application provides FPGA resource savings. The extent of resource savings depend on the granularity of the operations into which the application is decomposed. The thesis could also establish that runtime partial reconfiguration can be used to accelerate the computations in reconfigurable architectures with processor core like the Zynq-7000 platform. The achieved computational speed-up depends on factors like the number of hardware accelerators used for the computation and the used reconfiguration schedule. The thesis also highlights the power savings that may be achieved by executing computations in the reconfigurable fabric instead of the processor core.

3.8.2. Shihao Zhang: Delay Characterization in FPGA-based reconfigurable Systems

Betreuer: Dipl.-Inf. Michael Kochte, Dipl.-Inf. Michael Imhof

Abgabedatum: 03.12.2013

Abstract:

Runtime reconfigurable architectures accelerate the operation of a standard processor core by hardware accelerators implemented in Field Programmable Gate Arrays (FPGAs). Par- tial runtime reconfiguration allows the hardware accelerators to efficiently adapt to different computational tasks dynamically. Nowadays, the FPGAs from major vendors, such as Xilinx and Altera, support this feature,

including the Xilinx Virtex-5 FPGA family which is the implementation platform of this work.

Manufactured at 28 nm scaled technological node or lower, concerns rise about the impact of aging-related failure mechanisms on the modern generations of FPGAs. To detect degradation in the reconfigurable gate arrays, dedicated on- and offline test methods must be employed in the field. Design for dependability requires that the degradation is detected and localized, so that the degraded logic elements will not be used as a first choice in the reconfiguration.

This thesis presents the development and the evaluation of a delay characterization method for FPGA CLBs which comprise most of the FPGA logic elements. The purpose of FPGA delay characterization method in this work is to detect and localize the delay variance. This delay variance information may be used for achieving a speed optimized reconfiguration for a FPGA-based runtime system. Different delay characterization methods have been studied in this thesis for determining a suitable method to be implemented in the partial reconfigurable system. The delay characterization is performed in a part of area in the FPGA before a module is placed in this area to avoid the degraded portion. This thesis uses low level hardware description language to generate the fine-grained measurement units which can cover the target area. VHDL is used to generate the test wrapper, control circuit, and the circuit for communicating between the FPGA and the workstation. Several measurement techniques are used to evaluate the accuracy of the delay characterization method. Additionally, this thesis evaluates the temperature influence on the delay characterization.

The results show that this delay characterization method can compare the speed of logic elements in the partial runtime reconfiguration area with high accuracy. The degradation can be detected and localized. The results also show that this method can be adapted to different size and location, fitting in the partial runtime reconfigurable design. Twelve configurations are required to have a full coverage of all the CLBs in the area under test.

3.8.3. Siddharth Sunil Gosavi: Machine Learning Methods for Fault Classification

Betreuer: Dipl.-Inf. Laura Rodríguez Gómez

Abgabedatum: 24.04.2014

Abstract:

With the constant evolution and ever-increasing transistor densities in semiconductor technology, error rates are on the rise. Errors that occur on semiconductor chips can be attributed to permanent, transient or intermittent faults.

Out of these errors, once permanent errors appear, they do not go away and once intermittent faults appear on chips, the probability that they will occur again is high, making these two types of faults critical. Transient faults occur very rarely, making them non-critical. Incorrect classification during manufacturing tests in

case of critical faults, may result in failure of the chip during operational lifetime or decrease in product quality, whereas discarding chips with non-critical faults may result in unnecessary yield loss.

Existing mechanisms to distinguish between the fault types are mostly rule-based, and as fault types start manifesting similarly as we move to lower technology nodes, these rules become obsolete over time. Hence, rules need to be updated every time the technology is changed. Machine learning approaches have shown that the uncertainty can be compensated with previous experience. In our case, the ambiguity of classification rules can be compensated by storing past classification decisions and learn from those for accurate classification.

This thesis presents an effective solution to the problem of fault classification in VLSI chips using Support Vector Machine (SVM) based machine learning techniques.

3.9. Studienarbeit (Infotech Study Thesis)

3.9.1. Julian Oberacker: OASIS Testchip Gateway

Betreuer: Dipl.-Inf. Michael Kochte

Abgabedatum: 06.06.2014

Abstract:

Microelectronic circuits are aging during their operation. Decreasing structure sizes and increasing electric field strengths intensify the circuits' vulnerability for wearout and aging effects. Possible effects are for example changes in transistor parameters or defects on conductive paths. The idea of Online Failure Prediction for Microelectronic Circuits Using Aging Signatures (OASIS) is to detect changes in parameters by on-chip sensors and react accordingly to prevent system failures.

A testchip was designed to study aging effects and sensor mechanisms on an experimental basis. The chips consists of a 64 bit carry lookahead adder (CLA) and a 32 bit multiplier. Internal signals, so called "observation points", from those units can be monitored. A guard band generator with delay monitors and a delay Built In Self Test (BIST) can evaluate timing of the circuit. It is also possible to perform Faster-than-at-speed-tests.

An array of daisy-chained chips will be operated in a harsh environment to speed up aging. During the aging process, continuous test shall show the impact of wearout effects and prove the capability to detect those effects before the circuits fail. The experiments shall be configurable and programmable with a workstation. To be able to interface with the testchips, a gateway between workstation and chips under test is necessary. The task of this study thesis was to design and implement the gateway and the application interface for the workstation software.

4. Publikationen

4.1. Buchkapitel

4.1.1. Test und Diagnose

Wunderlich, H.-J.
in Siemers, C. and Sikora, A.(Ed.)
Taschenbuch Digitaltechnik, 3. neu bearbeitete Auflage 2014, pp. 262-285
ISBN: 978-3-446-43263-5, Carl Hanser Verlag GmbH & Co. KG
url: http://www.hanser-elibrary.com/isbn/9783446432635

4.2. Zeitschriften und Konferenzberichte

4.2.1. SAT-based Code Synthesis for Fault-Secure Circuits

Dalirsani, A., Kochte, M.A. and Wunderlich, H.-J.
Proc. 16th IEEE Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT'13), New York City, New York, USA, 2-4 October 2013, pp. 39-44
doi: http://dx.doi.org/10.1109/DFT.2013.6653580

This paper presents a novel method for synthesizing fault-secure circuits based on parity codes over groups of circuit outputs. The fault-secure circuit is able to detect all errors resulting from combinational and transition faults at a single node. The original circuit is not modified. If the original circuit is non-redundant, the result is a totally self-checking circuit. At first, the method creates the minimum number of parity groups such that the effect of each fault is not masked in at least one parity group. To ensure fault-secureness, the obtained groups are split such that no fault leads to silent data corruption. This is performed by a formal Boolean satisfiability (SAT) based analysis. Since the proposed method reduces the number of required parity groups, the number of two-rail checkers and the complexity of the prediction logic required for fault-secureness decreases as well. Experimental results show that the area overhead is much less compared to duplication and less in comparison to previous methods for synthesis of totally self-checking circuits. Since the original circuit is not modified, the method can be applied for fixed hard macros and IP cores.

4.2.2. Synthesis of Workload Monitors for On-Line Stress Prediction

Baranowski, R., Cook, A., Imhof, M.E., Liu, C. and Wunderlich, H.-J.
Proc. 16th IEEE Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT'13), New York City, New York, USA, 2-4 October 2013, pp. 137-142
doi: http://dx.doi.org/10.1109/DFT.2013.6653596

Stringent reliability requirements call for monitoring mechanisms to account for circuit degradation throughout the complete system lifetime. In this work, we efficiently monitor the stress experienced by the system as a result of its current workload. To achieve this goal, we construct workload monitors that observe the most relevant subset of the circuit's primary and pseudo-primary inputs and produce an accurate stress approximation. The proposed approach enables the timely adoption of suitable countermeasures to reduce or prevent any deviation from the intended circuit behavior. The relation between monitoring accuracy and hardware cost can be adjusted according to design requirements. Experimental results show the efficiency of the proposed approach for the prediction of stress induced by Negative Bias Temperature Instability (NBTI) in critical and near-critical paths of a digital circuit.

4.2.3. Accurate Multi-Cycle ATPG in Presence of X-Values

Erb, D., Kochte, M.A., Sauer, M., Wunderlich, H.-J. and Becker, B.
Proceedings of the 22nd IEEE Asian Test Symposium (ATS'13), Yilan, Taiwan, 18-21 November 2013
doi: http://dx.doi.org/10.1109/ATS.2013.53

Unknown (X) values in a circuit impair test quality and increase test costs. Classical n-valued algorithms for fault simulation and ATPG, which typically use a three- or four-valued logic for the good and faulty circuit, are in principle pessimistic in presence of X-values and cannot accurately compute the achievable fault coverage. In partial scan or pipelined circuits, X-values originate in non-scan flip-flops. These circuits are tested using multi-cycle tests. Here we present multi-cycle test generation techniques for circuits with X-values due to partial scan or other X-sources. The proposed techniques have been integrated into a multi-cycle ATPG framework which employs formal Boolean and quantified Boolean (QBF) satisfiability techniques to compute the possible signal states in the circuit accurately. Efficient encoding of the problem instance ensures reasonable runtimes. We show that in presence of X-values, the detection of stuck-at faults requires not only exact formal reasoning in a single cycle, but especially the consideration of multiple cycles for excitation of the fault site as well as propagation and controlled reconvergence of fault effects. For the first time, accurate deterministic ATPG for multi-cycle test application is supported for stuck-at faults. Experiments on ISCAS'89 and industrial circuits with X-sources show that this new approach increases the fault coverage considerably.

4.2.4. Securing Access to Reconfigurable Scan Networks

Baranowski, R., Kochte, M.A. and Wunderlich, H.-J.
Proceedings of the 22nd IEEE Asian Test Symposium (ATS'13), Yilan, Taiwan, 18-21 November 2013
doi: http://dx.doi.org/10.1109/ATS.2013.61

The accessibility of on-chip embedded infrastructure for test, reconfiguration, and debug poses a serious safety and security problem. Special care is required in the design and development of scan architectures based on IEEE Std. 1149.1 (JTAG), IEEE Std. 1500, and especially reconfigurable scan networks, as allowed by the upcoming IEEE P1687 (IJTAG). Traditionally, the scan infrastructure is secured after manufacturing test using fuses that disable the test access port (TAP) completely or partially. The fuse-based approach is efficient if some scan chains or instructions of the TAP controller are to be permanently blocked. However, this approach becomes costly if fine-grained access management is required, and it faces scalability issues in reconfigurable scan networks. In this paper, we propose a scalable solution for multi-level access management in reconfigurable scan networks. The access to protected registers is restricted locally at TAP-level by a sequence filter which allows only a precomputed set of scan-in access sequences. Our approach does not require any modification of the scan architecture and causes no access time penalty. Experimental results for complex reconfigurable scan networks show that the area overhead depends primarily on the number of allowed accesses, and is marginal even if this number exceeds the count of network's registers.

4.2.5. Verifikation Rekonfigurierbarer Scan-Netze

Baranowski, R., Kochte, M.A. and Wunderlich, H.-J.
Proc. 17. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV'14), Böblingen, Germany, 10-12 March 2014
url: https://cuvillier.de/de/shop/publications/6629-mbmv-2014

Rekonfigurierbare Scan-Netze, z. B. entsprechend IEEE Std. P1687 oder 1149.1-2013, ermöglichen den effizienten Zugriff auf On-Chip-Infrastruktur für Bringup, Debug, Post-Silicon-Validierung und Diagnose. Diese Scan-Netze sind oft hierarchisch und können komplexe strukturelle und funktionale Abhängigkeiten aufweisen. Bekannte Verfahren zur Verifikation von Scan-Ketten, basierend auf Simulation und struktureller Analyse, sind nicht geeignet, Korrektheitseigenschaften von komplexen Scan-Netzen zu verifizieren. Diese Arbeit stellt ein formales Modell für rekonfigurierbare Scan-Netze vor, welches die strukturellen und funktionalen Abhängigkeiten abbildet und anwendbar ist für Architekturen nach IEEE P1687. Das Modell dient als Grundlage für effizientes Bounded Model Checking von Eigenschaften, wie z. B. der Erreichbarkeit von Scan-Registern.

4.2.6. Bit-Flipping Scan - A Unified Architecture for Fault Tolerance and Offline Test

Imhof, M.E. and Wunderlich, H.-J.
Proc. Design, Automation and Test in Europe (DATE'14), Dresden, Germany, 24-28 March 2014
doi: http://dx.doi.org/10.7873/DATE.2014.206

Test is an essential task since the early days of digital circuits. Every produced chip undergoes at least a production test supported by on-chip test infrastructure to reduce test cost. Throughout the technology evolution fault tolerance gained importance and is now necessary in many applications to mitigate soft errors threatening consistent operation. While a variety of effective solutions exists to tackle both areas, test and fault tolerance are often implemented orthogonally, and hence do not exploit the potential synergies of a combined solution. The unified architecture presented here facilitates fault tolerance and test by combining a checksum of the sequential state with the ability to flip arbitrary bits. Experimental results confirm a reduced area overhead compared to a orthogonal combination of classical test and fault tolerance schemes. In combination with heuristically generated test sequences the test application time and test data volume are reduced significantly.

4.2.7. Non-Intrusive Integration of Advanced Diagnosis Features in Automotive E/E-Architectures

Abelein, U., Cook, A., Engelke, P., Glaß, M., Reimann, F., Rodríguez Gómez, L., Russ, T., Teich, J., Ull, D. and Wunderlich, H.-J.
Proc. Design, Automation and Test in Europe (DATE'14), Dresden, Germany, 24-28 March 2014
doi: http://dx.doi.org/10.7873/DATE.2014.373

With ever more complex automotive systems, the current approach of using functional tests to locate faulty components results in very long analysis procedures and poor diagnostic accuracy. Built-In Self-Test (BIST) offers a promising alternative to collect structural diagnostic information during E/E-architecture test. However, as the automotive industry is quite cost-driven, structural diagnosis shall not deteriorate traditional design objectives. With this goal in mind, the work at hand proposes a design space exploration to integrate structural diagnostic capabilities into an E/E-architecture design. The proposed integration is performed non-intrusively, i. e., the addition and execution of tests (a) does not affect any functional applications and (b) does not require any costly changes in the communication schedules.

4.2.8. Structural Software-Based Self-Test of Network-on-Chip

Dalirsani, A., Imhof, M.E. and Wunderlich, H.-J.
Proc. 32nd IEEE VLSI Test Symposium (VTS'14), Napa, California, USA, 13-17 April

2014
doi: http://dx.doi.org/10.1109/VTS.2014.6818754

Software-Based Self-Test (SBST) is extended to the switches of complex Network-on-Chips (NoC). Test patterns for structural faults are turned into valid packets by using satisfiability (SAT) solvers. The test technique provides a high fault coverage for both manufacturing test and online test.

4.2.9. Incremental Computation of Delay Fault Detection Probability for Variation-Aware Test Generation

Wagner, M. and Wunderlich, H.-J.
Proc. 19th IEEE European Test Symposium (ETS'14), Paderborn, Germany, 26-30 May 2014, pp. 1-6
doi: http://dx.doi.org/10.1109/ETS.2014.6847805

Large process variations in recent technology nodes present a major challenge for the timing analysis of digital integrated circuits. The optimization decisions of a statistical delay test generation method must therefore rely on the probability of detecting a target delay fault with the currently chosen test vector pairs. However, the huge number of probability evaluations in practical applications creates a large computational overhead. To address this issue, this paper presents the first incremental delay fault detection probability computation algorithm in the literature, which is suitable for the inner loop of automatic test pattern generation methods. Compared to Monte Carlo simulations of NXP benchmark circuits, the new method consistently shows a very large speedup and only a small approximation error.

4.2.10. Variation-Aware Deterministic ATPG

Sauer, M., Polian, I., Imhof, M.E., Mumtaz, A., Schneider, E., Czutro, A., Wunderlich, H.-J. and Becker, B.
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In technologies affected by variability, the detection status of a small-delay fault may vary among manufactured circuit instances. The same fault may be detected, missed or provably undetectable in different circuit instances. We introduce the first complete flow to accurately evaluate and systematically maximize the test quality under variability. As the number of possible circuit instances is infinite, we employ statistical analysis to obtain a test set that achieves a fault-efficiency target with an user-defined confidence level. The algorithm combines a classical path-oriented test-generation procedure with a novel waveformaccurate engine that can formally prove that a small-delay fault is not detectable and does not count towards fault efficiency. Extensive simulation results demonstrate the performance of the generated test sets for industrial circuits affected by uncorrelated and correlated variations.

4.2.11. Diagnosis of Multiple Faults with Highly Compacted Test Responses

Cook, A. and Wunderlich, H.-J.
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Defects cluster, and the probability of a multiple fault is significantly higher than just the product of the single fault probabilities. While this observation is beneficial for high yield, it complicates fault diagnosis. Multiple faults will occur especially often during process learning, yield ramp-up and field return analysis. In this paper, a logic diagnosis algorithm is presented which is robust against multiple faults and which is able to diagnose multiple faults with high accuracy even on compressed test responses as they are produced in embedded test and built-in self-test. The developed solution takes advantage of the linear properties of a MISR compactor to identify a set of faults likely to produce the observed faulty signatures. Experimental results show an improvement in accuracy of up to 22 % over traditional logic diagnosis solutions suitable for comparable compaction ratios.

4.2.12. Resilience Articulation Point (RAP): Cross-layer Dependability Modeling for Nanometer System-on-chip Resilience

Herkersdorf, A., Aliee, H., Engel, M., Glaß, M., Gimmler-Dumont, C., Henkel, J., Kleeberger, V.B., Kochte, M.A., Kühn, J.M., Mueller-Gritschneder, D., Nassif, S.R., Rauchfuss, H., Rosenstiel, W., Schlichtmann, U., Shafique, M., Tahoori, M.B., Teich, J., Wehn, N., Weis, C. and Wunderlich, H.-J.
Elsevier Microelectronics Reliability Journal (In press), Vol. 54(6-7), June-July 2014, pp. 1066-1074, doi: http://dx.doi.org/10.1016/j.microrel.2013.12.012

The Resilience Articulation Point (RAP) model aims at provisioning researchers and developers with a probabilistic fault abstraction and error propagation framework covering all hardware/software layers of a System on Chip. RAP assumes that physically induced faults at the technology or CMOS device layer will eventually manifest themselves as a single or multiple bit flip(s). When probabilistic error functions for specific fault origins are known at the bit or signal level, knowledge about the unit of design and its environment allow the transformation of the bit-related error functions into characteristic higher layer representations, such as error functions for data words, Finite State Machine (FSM) state, macro-interfaces or software variables. Thus, design concerns at higher abstraction layers can be investigated without the necessity to further consider the full details of lower levels of design. This paper introduces the ideas of RAP based on examples of radiation induced soft errors in SRAM cells, voltage variations and sequential CMOS logic. It shows by example how probabilistic bit flips are systematically abstracted and propagated towards higher abstraction levels up to the application software layer, and how RAP can be used to parameterize architecture-level resilience methods.

4.2.13. Exact Logic and Fault Simulation in Presence of Unknowns

Erb, D., Kochte, M.A., Sauer, M., Hillebrecht, S., Schubert, T., Wunderlich, H.-J. and Becker, B.
ACM Transactions on Design Automation of Electronic Systems (TODAES)
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doi: http://dx.doi.org/10.1145/2611760

Logic and fault simulation are essential techniques in electronic design automation. The accuracy of standard simulation algorithms is compromised by unknown or X-values. This results in a pessimistic overestimation of X-valued signals in the circuit and a pessimistic underestimation of fault coverage. This work proposes efficient algorithms for combinational and sequential logic as well as for stuck-at and transition-delay fault simulation that are free of any simulation pessimism in presence of unknowns. The SAT-based algorithms exactly classifiy all signal states. During fault simulation, each fault is accurately classified as either undetected, definitely detected, or possibly detected. The pessimism with respect to unknowns present in classic algorithms is thoroughly investigated in the experimental results on benchmark circuits. The applicability of the proposed algorithms is demonstrated on larger industrial circuits. The results show that, by accurate analysis, the number of detected faults can be significantly increased without increasing the test-set size.

4.2.14. GUARD: GUAranteed Reliability in Dynamically Reconfigurable Systems

Zhang, H., Kochte, M.A., Imhof, M.E., Bauer, L., Wunderlich, H.-J. and Henkel, J.
Proc. 51st ACM/EDAC/IEEE Design Automation Conference (DAC'14), San Francisco, California, USA, 1-5 June 2014, pp. 1-6, **HiPEAC Paper Award**
doi: http://dx.doi.org/10.1145/2593069.2593146

Soft errors are a reliability threat for reconfigurable systems implemented with SRAM-based FPGAs. They can be handled through fault tolerance techniques like scrubbing and modular redundancy. However, selecting these techniques statically at design or compile time tends to be pessimistic and prohibits optimal adaptation to changing soft error rate at runtime. We present the GUARD method which allows for autonomous runtime reliability management in reconfigurable architectures: Based on the error rate observed during runtime, the runtime system dynamically determines whether a computation should be executed by a hardened processor, or whether it should be accelerated by inherently less reliable reconfigurable hardware which can trade-off performance and reliability. GUARD is the first runtime system for reconfigurable architectures that guarantees a target reliability while optimizing the performance. This allows applications to dynamically chose the desired degree of reliability. Compared to related work with statically optimized fault tolerance techniques, GUARD provides up to 68.3 % higher performance at the same target reliability.

4.2.15. Advanced Diagnosis: SBST and BIST Integration in Automotive E/E Architectures

Reimann, F., Glaß, M., Teich, Jü., Cook, A., Rodríguez Gómez, L., Ull, D., Wunderlich, H.-J., Abelein, U. and Engelke, P.
Proc. 51st ACM/IEEE Design Automation Conference (DAC'14), San Francisco, California, USA, 1-5 June 2014, pp. 1-9, **HiPEAC Paper Award**
doi: http://dx.doi.org/10.1145/2593069.2602971

The constantly growing amount of semiconductors in automotive systems increases the number of possible defect mechanisms, and therefore raises also the effort to maintain a sufficient level of quality and reliability. A promising solution to this problem is the on-line application of structural tests in key components, typically ECUs. In this work, an approach for the optimized integration of both Software-Based Self-Tests (SBST) and Built-In Self-Tests (BIST) into E/E architectures is presented. The approach integrates the execution of the tests non-intrusively, i. e., it (a) does not affect functional applications and (b) does not require costly changes in the communication schedules or additional communication overhead. Via design space exploration, optimized implementations with respect to multiple conflicting objectives, i. e., monetary costs, safety, test quality, and required execution time are derived.

4.2.16. A New Hybrid Fault-Tolerant Architecture for Digital CMOS Circuits and Systems

Tran, D.A., Virazel, A., Bosio, A., Dilillo, L., Girard, P., Pravossoudovich, S. and Wunderlich, H.-J.
Journal of Electronic Testing: Theory and Applications (JETTA)
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doi: http://dx.doi.org/10.1007/s10836-014-5459-3

This paper presents a new hybrid fault-tolerant architecture for robustness improvement of digital CMOS circuits and systems. It targets all kinds of errors in combinational part of logic circuits and thus, can be combined with advanced SEU protection techniques for sequential elements while reducing the power consumption. The proposed architecture combines different types of redundancies: information redundancy for error detection, temporal redundancy for soft error correction and hardware redundancy for hard error correction. Moreover, it uses a pseudo-dynamic comparator for SET and timing errors detection. Besides, the proposed method also aims to reduce power consumption of fault-tolerant architectures while keeping a comparable area overhead compared to existing solutions. Results on the largest ISCAS'85 and ITC'99 benchmark circuits show that our approach has an area cost of about 3 % to 6 % with a power consumption saving of about 33 % compared to TMR architectures.

4.2.17. A-ABFT: Autonomous Algorithm-Based Fault Tolerance for Matrix Multiplications on Graphics Processing Units

Braun, C., Halder, S. and Wunderlich, H.-J.
Proc. of The 44th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN'14), Atlanta, Georgia, USA, 23-26 June 2014, pp. 443-454
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Graphics processing units (GPUs) enable large-scale scientific applications and simulations on the desktop. To allow scientific computing on GPUs with high performance and reliability requirements, the application of software-based fault tolerance is attractive. Algorithm-Based Fault Tolerance (ABFT) protects important scientific operations like matrix multiplications. However, the application to floating-point operations necessitates the runtime classification of errors into inevitable rounding errors, allowed compute errors in the magnitude of such rounding errors, and into critical errors that are larger than those and not tolerable. Hence, an ABFT scheme needs suitable rounding error bounds to detect errors reliably. The determination of such error bounds is a highly challenging task, especially since it has to be integrated tightly into the algorithm and executed autonomously with low performance overhead.

In this work, A-ABFT for matrix multiplications on GPUs is introduced, which is a new, parallel ABFT scheme that determines rounding error bounds autonomously at runtime with low performance overhead and high error coverage.

4.2.18. Area-Efficient Synthesis of Fault-Secure NoC Switches

Dalirsani, A., Kochte, M.A. and Wunderlich, H.-J.
Proc. of the 20th IEEE International On-Line Testing Symposium (IOLTS'14), Platja d'Aro, Catalunya, Spain, 7-9 July 2014, pp. 13-18
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Unknown or X-values during test application may originate from uncontrolled sequential cells or macros, from clock or A/D boundaries or from tri-state logic. The exact identification of X-value propagation paths in logic circuits is crucial in logic simulation and fault simulation. In the first case, it enables the proper assessment of expected responses and the effective and efficient handling of X-values during test response compaction. In the second case, it is important for a proper assessment of fault coverage of a given test set and consequently influences the efficiency of test pattern generation. The commonly employed n-valued logic simulation evaluates the propagation of X-values only pessimistically, i.e. the X-propagation paths found by n- valued logic simulation are a superset of the actual propagation paths. This paper presents an efficient method to overcome this pessimism and to determine accurately the set of signals which carry an X-value for an input pattern. As examples, it investigates the influence of this pessimism on the two applications X-masking and stuck-at fault coverage assessment. The experimental results on benchmark and industrial circuits assess the pessimism of classic algo-

rithms and show that these algorithms significantly overestimate the signals with X-values. The experiments show that overmasking of test data during test compression can be reduced by an accurate analysis. In stuck-at fault simulation, the coverage of the test set is increased by the proposed algorithm without incurring any overhead.

4.2.19. SAT-based ATPG beyond stuck-at fault testing

Hellebrand, S. and Wunderlich, H.-J.
it - Information Technology
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To cope with the problems of technology scaling, a robust design has become desirable. Self-checking circuits combined with rollback or repair strategies can provide a low cost solution for many applications. However, standard synthesis procedures may violate design constraints or lead to sub-optimal designs. The SAT-based strategies for the verification and synthesis of self-checking circuits presented in this paper can provide efficient solutions.

4.2.20. Multi-Level Simulation of Non-Functional Properties by Piecewise Evaluation

Hatami, N., Baranowski, R., Prinetto, P. and Wunderlich, H.-J.
ACM Transactions on Design Automation of Electronic Systems (TODAES)
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doi: http://dx.doi.org/10.1145/2647955

As the technology shrinks, nonfunctional properties (NFPs) such as reliability, vulnerability, power consumption, or heat dissipation become as important as system functionality. As NFPs often influence each other, depend on the application and workload of a system, and exhibit nonlinear behavior, NFP simulation over long periods of system operation is computationally expensive, if feasible at all.

This article presents a piecewise evaluation method for efficient NFP simulation. Simulation time is divided into intervals called evaluation windows, within which the NFP models are partially linearized. High-speed functional system simulation is achieved by parallel execution of models at different levels of abstraction. A trade-off between simulation speed and accuracy is met by adjusting the size of the evaluation window.

As an example, the piecewise evaluation technique is applied to analyze aging caused by two mechanisms, namely Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI), in order to identify reliability hotspots. Experiments show that the proposed technique yields considerable simulation speedup at a marginal loss of accuracy.

4.2.21. Adaptive Bayesian Diagnosis of Intermittent Faults

Rodríguez Gómez, L., Cook, A., Indlekofer, T., Hellebrand, S. and Wunderlich, H.-J.
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With increasing transient error rates, distinguishing intermittent and transient faults is especially challenging. In addition to particle strikes relatively high transient error rates are observed in architectures for opportunistic computing and in technologies under high variations. This paper presents a method to classify faults into permanent, intermittent and transient faults based on some intermediate signatures during embedded test or built-in self-test.

Permanent faults are easily determined by repeating test sessions. Intermittent and transient faults can be identified by the amount of failing test sessions in many cases. For the remaining faults, a Bayesian classification technique has been developed which is applicable to large digital circuits. The combination of these methods is able to identify intermittent faults with a probability of more than 98 %.

4.3. Workshop-Beiträge

4.3.1. A-ABFT: Autonomous Algorithm-Based Fault Tolerance on GPUs

Braun, C., Halder, S. and Wunderlich, H.-J.
International Workshop on Dependable GPU Computing, in conjunction with the ACM/IEEE DATE'14 Conference, Dresden, Germany, 28 March 2014

General-purpose computations on graphics processing units (GPUs) enable large-scale scientific applications and simulations on the desktop. Such applications typically have high performance and reliability requirements. For GPUs, which are still designed for the graphics mass-market, hardware-based fault tolerance measures often do not have the highest priority, which makes the application of appropriate software-based fault tolerance mandatory.

Algorithm-based Fault Tolerance (ABFT) allows the efficient and effective protection of important kernels from scientific computing. Some ABFT schemes have already been adapted for GPU architectures. However, due to roundoff error introduced by floating-point arithmetic, ABFT requires the determination of tight error bounds for the error detection. The determination of such error bounds is a highly challenging task.

In this work, we introduce A-ABFT for GPUs, a new parallel ABFT scheme that determines appropriate error bounds for the checksum comparison step autonomously and which therefore enables the transparent operation of ABFT without any user interaction.


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